An Ultra-Low-Power Low-Data-Rate Neural Recording System with Adaptive Spike Detection

Donghwi Kim, Milutin Stanaćević and Ridha Kamoua
Department of Electrical and Computer Engineering
Stony Brook University
Stony Brook, New York 11794–2350, USA
Email: {dhkim, milutin, and ridha}@ece.sunysb.edu

Zachary Mainen
Cold Spring Harbor Laboratory
Cold Spring Harbor, New York 11724, USA
Email: mainen@cshl.edu

***Abstract*— A design of small, ultra-low-power, low-data rate, wireless 32-channel neural recording system for small animal head-stage is presented. A neural pre-amplifier has low-input-referred-noise of 1.95μV_{rms} and consumes 53.6μW. To enable digital telemetry with optimized bandwidth under size and power constraint for small-animal headstage, we propose to separately record spikes and local-field potentials. An adaptive spike detector using absolute value algorithm accompanied with 7th-order all-pass delay filter provides accurate on-chip acquisition of spike waveform in duration of 2ms. A low-power 10-bit and 5-bit resolution A/D converters running at 22$Ksamples/s$ for active spikes and 200$samples/s$ for local field potential, respectively, can be integrated with the proposed system. Using adaptive bandwidth control, we achieve reduction of data-rate up to seven times which provides compatibility to 1$Mbps$ Ultra Low Power Bluetooth technology. Total power consumption of single channel excluding ADCs is 109.58μW in 3.3V power supply.**

I. Introduction

Recording and collection of large population of neural signals in small animal is required to investigate for bio-physiological activities in central and/or peripheral nervous system. There is a need for a system able to record all informative data and communicate the gathered data with a recording station in such a way that animal movement is restricted in minimal way.

Existing systems for multi-channel recording mainly use analog headstage requiring a number of wires equal to the number of channels, leading to restriction of movement and poor scalability. Most of these systems use pre-amplifier and front-end filtering to improve the signal-to-noise ratio before transmission to a remote data logger. Wireless transmitting devices might solve that problem, but current generations based on analog multiplexing also scale poorly and are susceptible to noise [1], [2]. The design of a headstage with on-chip analog-to-digital conversion would enable digital telemetry of neural signals in their entirety, however high-data-rate in multi-channel implementation is concern and efficient control of bandwidth is necessary. To control the bandwidth and transmit all informative data, we need to transmit effective spike shapes accurately at higher sampling rate, enabling off-chip digital spike sorting, while local field potentials can be acquired at lower resolution and lower sampling rate.

We are investigating a design of wireless VLSI micro-system for recording of neural signals from array of micro-electrodes mounted on a head of a rat-like small animal. The head-stage would interface with an Ultra Low Power Bluetooth technology [3], previously called Wibree, which consumes only a fraction of the power of the classic Bluetooth, can be powered by a small and light button cell battery and supports data-rate of 1Mbps. A higher resolution ADC can be utilized whenever an active spike is detected, and a lower resolution ADC is adequate for recording of local field potential (LFP). The chip-on-board technology would be used for volume reduction and would enable interface to different sensor arrays.

We have considered 32-channel analog neural recording system integrated together with an adaptive spike detector using absolute value algorithm in 0.6μm CMOS technology.

II. Ultra-Low-Power Low-Data-Rate System Design

Figure 1 shows single channel of the system block diagram for the proposed ultra-low-power, low-data-rate neural recording system. It consists of a pre-amplifier, 7th order all-pass delay filter, an adaptive spike detector using absolute value algorithm, high-pass filter, low-pass amplifiers, 10-bit ADC and 5-bit ADC. In the pre-amplifier, since the peak-to-peak voltage of input spike train and LFP, in case of removal of random DC offset, are micro-range (at most 2mV_{pp}, typically 200μV_{pp} for spikes and about 2mV_{pp} for LFP), neural signals from a electrode are amplified fifty times only in the range from 1Hz to 7kHz. This is because the linear range of the all-pass filter and the adaptive spike detector (ASD) in the figure is set to 200mV_{pp}. A high-pass filter (HPF) is used for selection of only spike bandwidth. ASD is to adaptively set a detection threshold by a multiplication factor which would be adjusted high or low by external digital signal. A linear phase all-pass delay filter allows the previously amplified spikes to preserve the shape of waveforms in band of interests with certain amount of delay. Two low-pass filter amplifiers (LPF-AMPs) before two ADCs are not only to enlarge input dynamic range of ADC but also work as anti-aliasing filters for the digitization (A 7kHz band-width LPF-AMP for active spikes, and 100Hz band-width LPF-AMP for LFP). For the 10-bit ADC, a low-power, small-size, ratio-independent algorithmic-type ADC [4] can be considered for this application. It will be activated by the one bit spike acknowledge signal from

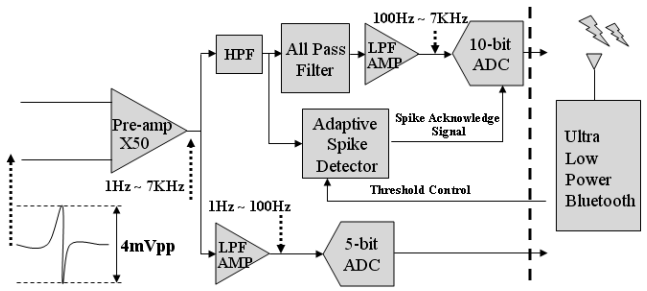

Fig. 1. *A single-channel system diagram for the proposed adaptive neural recording system.*

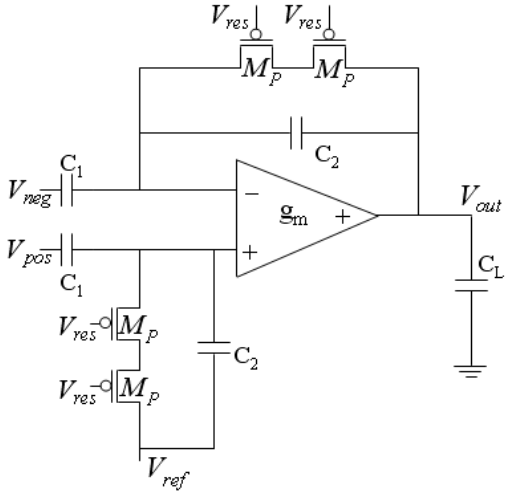

Fig. 2. *Schematic diagram for a low-input-referred-noise pre-amplifier.*

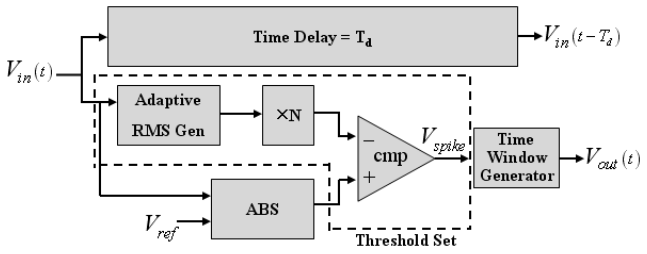

Fig. 3. *A block diagram of the adaptive spike detector using absolute value algorithm.*

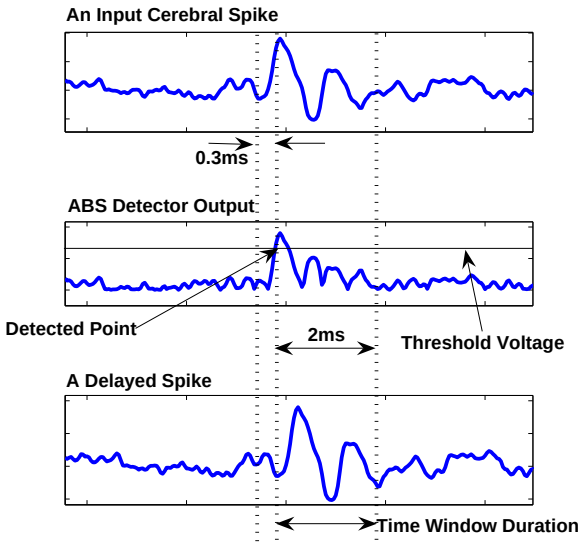

Fig. 4. *Typical specifications for a cerebral spike from a rat. This in-vivo data was acquired by Cold Spring Harbor Lab., New York. The threshold value was set by the adaptive spike detection algorithm in MATLAB.*

the ASD. Whenever an active spike signal is detected the ADC runs at $22Ksamples/s$. For the 5-bit ADC, a successive approximation-type ADC running at $200samples/s$ can be considered for recording of LFP. Since it is low resolution only few pico-farads capacitors will be utilized for a binary-weighted capacitor array. Digitized data will be processed in the off-chip and interfaced with Ultra Low Power Bluetooth chip for wireless transmission.

A. Pre-Amplifier Design

Figure 2 shows the structure of designed pre-amplifier which is based on our previous design [5]. Pre-amplifier is especially designed for taking only neural action potentials which have frequency components in the range of 1Hz - 7kHz. The bandwidth is set by $g_m/A_M C_L$, where g_m is the transconductance of the operational transconductance amplifier (OTA), A_M is midband gain set by C_1/C_2, and C_L is load capacitance seen from output of the pre-amplifier. Low cut-off frequency is determined by $1/(2\pi 2R_P C_2)$ using resistance (R_P) of a pseudo PMOS element, up to the order of $10^{13}\Omega$ depending on a biasing voltage (V_{RES}). For design of OTA in pre-amplifier, wide-swing current-mirror operational amplifier is utilized with consideration of high gain, stability, and low-noise properties. By maximizing the gain of OTA, the effect of parasitic capacitances at the input of OTA could be reduced. It also makes possible to use smaller C1 and C2 capacitors to set a gain. Capacitors C_1, C_2 are set to 7.5pF, 150fF respectively. Since the tolerable noise level for 10-bit ADC operating in 1V reference is 488.28μV, the input-referred noise of pre-amplifier is set to 1.95μV_{rms}. This would not overwhelm active signals in the channel gain of $250V/V$.

B. Adaptive Spike Detector using Absolute Value Algorithm

Iyad and Patrick [6] have compared spike-detection algorithms for wireless brain-machine interfaces. They found that, in systems with limited computational resources, taking the absolute value of the neural signal before applying a threshold is just as effective for detecting spikes as applying more elaborate energy-based detectors using digital signal processing techniques. Based on their research, Figure 3 presents a proposed block diagram for an analog spike detector using an absolute value algorithm. It comprises four main building blocks: adaptive real-time threshold set block, absolute value block (ABS), Time delay block, and time window generator block. The adaptive real-time threshold set block was first introduced and validated by Harrison [7], [8]. It performs spike detection using a specified multiple (N in Figure 3, usually 3 to

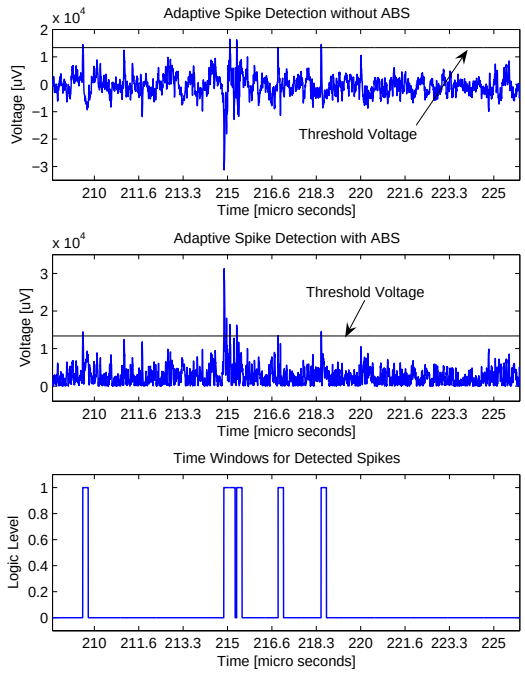

Fig. 5. *Comparative views of adaptive spike detector without ABS (figure in the first row) and with ABS (figure in the second row). The detected spikes allow to produce time window signals (figure in the third row).*

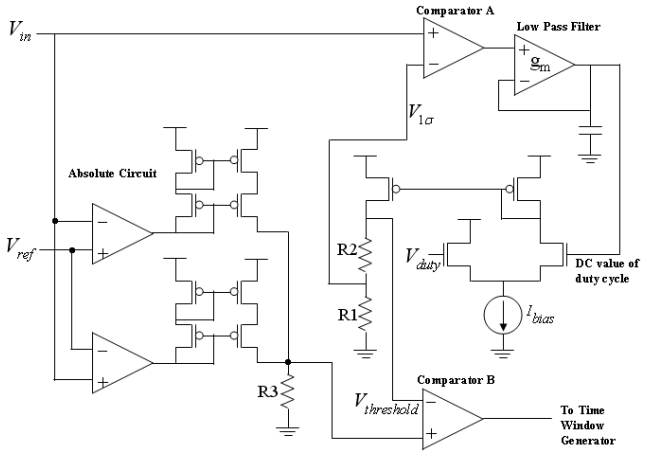

Fig. 6. *A schematic of the adaptive spike detector using absolute value. An absolute value circuit was adopted to implement absolute value algorithm and adaptive threshold set scheme was from Harrison's [7], [8].*

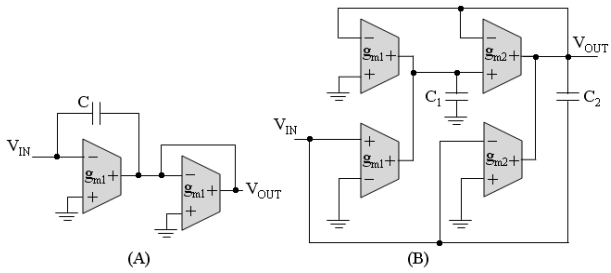

Fig. 7. *A first-order (A) and second-order (B) all-pass delay filter circuit.*

7) of the background noise rms value. ABS block generates absolute value with respect to common mode reference for input neural signal. Time window generator block produces 1-bit digital enable signals for $2msec$, that is required time period for successful recording of an active spike shape. Time delay block makes $0.3msec$ delay time without loss of any frequency component. It allows to record the entire waveform of detected spike. The delay is set based on observation that an active spike typically has $0.3msec$ time period before its waveform first reaches the estimated threshold value, and it would be already late to record a shape of neural spike even as soon as the adaptive detector recognizes it as a neural spike. Figure 4 shows the specifications for a detected neural spike.

Figure 5 represents waveforms through the proposed adaptive spike detector without/with the ABS in Matlab simulation, and plots the generated time window signals. As in the first row of the figure, it is observed that some negative spikes might be created by a cell as well as positive spikes. It can be detected by ABS (in the second row of the figure) and creates a time window for $2msec$ after delay time of $0.3msec$ as in the third row of the figure. If a consecutive spike hit the threshold during generating of $2msec$ time window for the previous one time window generator will reset the timer and extend $2msec$ more from the moment.

1) Circuits for Adaptive Spike Detector: Figure 6 depicts implemented adaptive spike detector with the ABS. Adaptive threshold set block in right side of the figure 6 follows the circuit in [7], [8]. Comparator A is used in feedback loop and setting $V_{1\sigma}$ to the rms level of the input waveform. This voltage is amplified by a constant level (usually 3 to 7) by the ratio of R1 and R2. The voltage, $V_{threshold}$, results in adaptive threshold voltage. Absolute value circuit consists of two identical operational transconductance amplifiers (OTA) and two identical PMOS cascode mirrors, rather than one OTA with one PMOS current source and one NMOS current sink introduced in [9], to reduce a current mismatch error between NMOS and PMOS.

2) All-pass Delay Filter Design: All-pass time delay filter is designed to make $0.3msec$ delay without loss of spike waveform. A 7th order filter is chosen to set $0.3msec$ delay and comprises one first-order and three second-order all-pass filters in a series starting with the first-order filter. A structure for discrete version of higher order all-pass filter and its coefficients was introduced in [10]. We convert it to its gm-C version for VLSI implementation. Figure 7 presents gm-C version of first-order and second-order all-pass filter structure. Their transfer functions are summarized in equation (1) and (2) respectively.

$$H_{1st}(s) = \frac{s - \frac{g_{m1}}{C}}{s + \frac{g_{m1}}{C}} \tag{1}$$

$$H_{2nd}(s) = \frac{s^2 - \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{2}$$

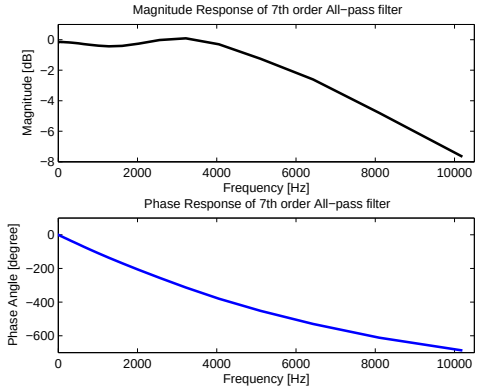

Fig. 8. *Magnitude and phase response of simulated 7th-order all-pass filter in Cadence.*

TABLE I

SUMMARY OF SIMULATED POWER CONSUMPTION.

Building Block	Power consumption
Pre-amplifier	53.6μW
Adaptive spike detector	19.8μW
7th-order all-pass filter	0.54μW
Two LPF-AMPs and one HPF	35.64μW
Total consumption	109.58μW

Designed 7th order all-pass filter has $0.3msec$ delay up to 3dB bandwidth of 7kHz and it has almost linear phase up to the bandwidth. Figure 8 presents the simulated magnitude and phase response of all-pass filter in Cadence. All three second-order filters use 1 pF capacitors and the very first filter, first-order filter, uses 2 pF capacitor. All designed transconductors have $200mV$ linear range and their transconductance range from $2nA/V$ to $15nA/V$.

III. SIMULATED POWER CONSUMPTION AND DATA-RATE IMPROVEMENT

The designed circuits were simulated in 3.3V power supply using Cadence SpectreS simulator. Table I summaries the power consumption of each simulated block. The total power consumption of single channel system excluding ADCs is 46.14μW.

It is known that spike firing rate for small animals is distributed widely from $10spikes/sec$ to $90spikes/sec$ [11]. The spike firing rate from cerebral cortex of a rat is $50\sim60spikes/sec$. Table II summarizes the tremendously reduced data-rate by the proposed adaptive spike detection system. Without adaptive system with the same specifications, the produced data-rate is 7040000bps. We manage to reduce the data-rate almost 7 times with the proposed system.

TABLE II

PRODUCED DATA-RATE BY PROPOSED SYSTEM.

	Ch.	Occupation	Fs	Resolution.	Data-Rate
Spikes	32	0.14	$22Ks/s$	10bit	985600bps
Others	32	1	$200s/s$	5bit	32000bps

The occupation rate of spikes in one second in Table II was calculated by an assumption that maximum firing rate is $70spikes/sec$. Since recording time for each spike is $2msec$ the percentage occupied by spikes in one second is 14%. The total produced data-rate is 1017600bps (985600bps+32000bps in Table II) which is less than $1Mbps$ (1048576bps). It allows us to transmit 32 channel neural data accurately using $1Mbps$ Ultra Low Power Bluetooth technology.

IV. CONCLUSIONS

This work presents a design of ultra-low-power, low-data-rate, wireless head-stage of small animals, 32-channel neural recording system. It is compatible with Ultra Low Power Bluetooth technology using button cell battery. The proposed 32-channel adaptive neural recording system would be integrated together with ADCs into a $3mm$ by $3mm$ chip area in 0.6μm CMOS process.

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