Current-mode Preamplifier for Response Measurement of Semiconductor Scintillator

Xiao Yun, Milutin Stanaćević, Vladis Kuzminsky and Mikhail Gouzman
Department of Electrical and
Computer Engineering
Stony Brook University
NY, USA
Email: xyun, milutin, slava, mig@ece.sunysb.edu

Abstract— A design of front-end preamplifier for measurement of optical response of photo-detector registering light produced by semiconductor scintillator is presented. The designed preamplifier is based on a current mode, regulated cascode (RGC) structure. A comparison with a previously reported common gate (CG) structure is provided. The experimental prototype was designed in 0.5μm CMOS process. With a 5 V power supply, total power consumption of a chip is $7.5m$W. With 50 pF input capacitance and 100 nA leakage current of interfaced photo-detector, the equivalent noise charge (ENC) is 8000.

Fig. 1.   Block diagram

I. INTRODUCTION

The detection of nuclear radiation is important part of prevention of terrorist threats. Due to high sensitivity of current radiation detectors, reduction of "false alarms" becomes critical. The proposed three-dimensional (3D) integration of scintillation-type semiconductor detector pixels provides accurate spectroscopic resolution for isotope discrimination and an accurate determination of the direction to source at the same time [1]. In novel scintillation-type semiconductor detector high energy radiation produces electron-hole pairs in a direct-gap semiconductor material that subsequently undergo interband recombination, producing infrared light to be registered by a photo-detector. To measure the optical response of pixelized detector, an application specific integrated circuit has to be designed.

The signal generated by the photo-detector represents a current pulse that is around 10 ns wide. The parasitic capacitance to ground of the photo-detector imposes the most stringent constraint in the design. The value of parasitic capacitance, for the pixel size of $1mm$ x $1mm$ is estimated to be 50 pF. The large parasitic capacitance gives uniqueness to the specifications imposed on the sensing circuitry and requires development of novel circuit techniques to relax the effect of input parasitic capacitance. The current magnitude of the pulse is determined by the charge produced by photo-detector. The sensitivity of the sensing circuitry should be on the order of 10,000 electrons. The leakage current is estimated to be 100 nA.

II. DESIGN OF A CURRENT MODE PREAMPLIFIERS

According to the specific application requirement, the front-end input stage needs to be a very critical low-noise and large-bandwidth 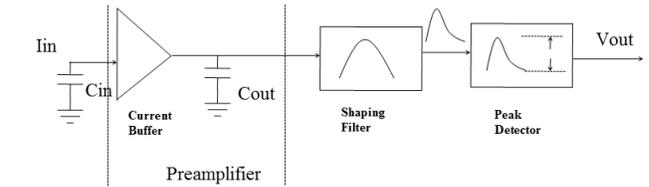circuit. A current mode preamplifier is selected over its voltage mode counterpart, because it avoids charging and discharging of the parasitic capacitors to high-voltage levels and keeps the internal nodes at low-impedance values [2]. Another advantage of using current mode preamplifier is that it is more easily adopted with large detector leakage current.

The preamplifier in this design is implemented as a robust current-to-voltage converter based on a regulated cascode common gate (RGC) structure. The input current pulse first flows through a current buffer, which isolates the large input capacitance, and then integrates on a small capacitor. A comparison between this design and a previously reported design [3] based on a common gate configuration is also provided. The output of the preamplifier is first shaped with a semi-gaussian pulse shaping filter and then further processed with a peak detector before it is being digitized and read out. The system block diagram is shown in figure 1.

A. Common gate configuration

The common gate (CG) configuration is shown in figure 2. C_{in} is the detector parasitic capacitance, which is 50 pF in our design. C_{out} is the parasitic capacitance at the output node.

With the help of a small-signal analysis, the input impedance of the CG configuration is:

$$Z_{in,CG} = \frac{1}{g_{m1}} \quad (1)$$

For simplicity, the circuit can be modeled as a two poles system, with one pole at the input node, the other at the output. Transfer function of the CG structure can be described as follows:
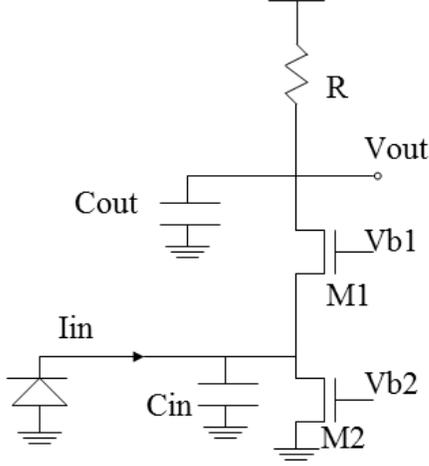
Fig. 2. CG circuit schematic

Fig. 3. RGC circuit schematic

$$H_{CG}(s) = \frac{Vout(s)}{Iin(s)} = \frac{R}{(\frac{C_{in}}{g_{m1}}s + 1)(RC_{out}s + 1)} \quad (2)$$

To get an understanding of the noise performance, noise has to be integrated at the output and compared with the output signal. The total integrated output noise is

$$V_{n,out,tot}^2 = \frac{C_{in}I_{n,M1}^2 R}{4C_{out}[C_{in} + g_{m1}RC_{out}]}$$
$$+ \frac{(I_{n,M2}^2 + 2qI_0)R^2 g_{m1}}{4[C_{in} + g_{m1}RC_{out}]}$$
$$+ \frac{kT}{C_{out}} \quad (3)$$

where $I_{n,M1}$, $I_{n,M2}$ and $I_{n,R}$ are noise current sources of $M1$, $M2$ and R respectively. I_0 is the leakage current of the detector. Note that during the above analysis, we ignore the input referred voltage noise. That is because the input impedance seen into the source of $M1$ is typically very small.

The input signal is modeled as a fast current pulse with 2ns rising time, 8ns falling time. It is a good estimation for the specific detector in our application. Assuming the input pole is much greater than the output pole, and a very large R is implemented, the signal output in response to a single electron can be expressed approximately as:

$$V_{s,out} = \frac{q}{C_{out}} \quad (4)$$

where q is the charge of a single electron.

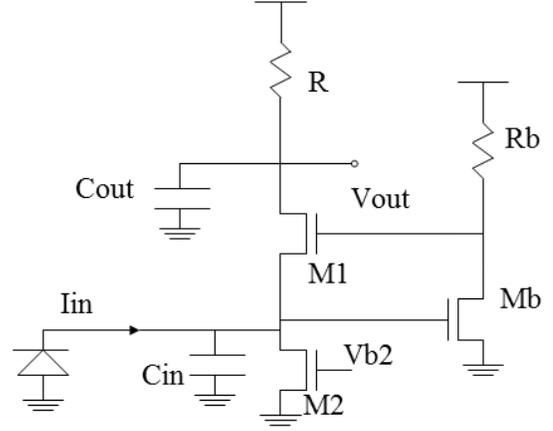The equivalent noise charge (ENC) can be calculated by

dividing the above two equations.

$$ENC^2 = \frac{C_{in}kT\gamma}{q^2}$$
$$+ \frac{(2kT\gamma g_{m2} + qI_0)RC_{out}}{2q^2}$$
$$+ \frac{kTC_{out}}{q^2} \quad (5)$$

assuming $C_{in} \ll g_{m1}RC_{out}$. γ is thermal noise factor.

The above equation reveals two problems of the CG structure. First, it requires a relatively large g_{m1}. This is a direct impact of the large input capacitance, since a smaller g_{m1} limits the bandwidth of the current buffer, and fewer charge is integrated on the output capacitance. A large g_{m1} can be achieved with either wider transistor or larger biasing current. The former increases the gate capacitance of $M1$, which in turn, adds up to the input capacitance. The latter obviously leads to a higher power consumption. Second, it shows little flexibility in the design of CG preamplifier. The only parameter under control is g_{m2}. However, for a fixed bias current, g_{m2} is reduced only at the cost of voltage headroom.

B. Regulated cascode configuration

The regulated cascode (RGC) common gate circuit schematic is shown in figure 3. With M_b and R_b, the input impedance is boosted to $1/[g_{m1}(g_{mb}R_b + 1)]$ instead of $1/g_{m1}$. A similar transfer function can be derived as:

$$H_{RGC}(s) = \frac{Vout(s)}{Iin(s)} = \frac{R}{(\frac{C_{in}}{g_{m1}(g_{mb}Rb+1)}s + 1)(RC_{out}s + 1)} \quad (6)$$

It is obvious that with $(g_{mb}R_b + 1)$ times smaller input impedance, the RGC configuration provides better isolation of the input parasitic capacitance [4].

The same method is used to calculate the total integrated output noise,

$$
\begin{aligned}
V_{n,out,tot}^2 &= \frac{C_{in}I_{n,Mb}^2 R(g_{m1}(g_{mb}R_b+1))^2/g_{mb}^2}{4C_{out}[C_{in}+g_{m1}(g_{mb}R_b+1)RC_{out}]} \\
&+ \frac{(C_{gs1}+C_{gdb})I_{n,M1}^2 R(g_{mb}R_b+1)^2}{4C_{out}[C_{in}+g_{m1}(g_{mb}R_b+1)RC_{out}]} \\
&+ \frac{(I_{n,M2}^2+2qI_0)R^2 g_{m1}(g_{mb}R_b+1)}{4[C_{in}+g_{m1}(g_{mb}R_b+1)RC_{out}]} \\
&+ \frac{kT}{C_{out}} \quad (7)
\end{aligned}
$$

where C_{gs1} is the gate-source capacitance of $M1$, C_{gdb} is the gate-drain capacitance of Mb. It is observed that noise contributed from $M1$ is now related with a much smaller capacitance $C_{gs1}+C_{gdb}$, and high frequency noise associated with the large input capacitance is now related with Mb.

If $g_{m1}(1+R_b g_{mb})$ and R are large enough, the output signal can still be expressed as equation (4). The equivalent noise charge (ENC) can be calculated as:

$$
\begin{aligned}
ENC^2 &= \frac{C_{in}kT\gamma g_{m1}(g_{mb}R_b+1)}{q^2 g_{mb}} \\
&+ \frac{(C_{gs1}+C_{gdb})kT\gamma(g_{mb}R_b+1)}{q^2} \\
&+ \frac{(2kT\gamma g_{m2}+qI_0)RC_{out}}{2q^2} \\
&+ \frac{kTC_{out}}{q^2} \quad (8)
\end{aligned}
$$

assuming $C_{in} \ll g_{m1}(g_{mb}R_b+1)RC_{out}$.

Compared to CG structure, the RGC structure greatly relaxes the requirement of g_{m1}, and thus reduces power consumption. The contribution from $M2$ can be reduced as, in RGC, it has a smaller biasing current which leads to smaller g_{m2}. The main noise component, first term in the above equation, can be controlled by having a bigger g_{mb} and smaller g_{m1}. Theoretically, $C_{gsb} \approx C_{in}$ [4] for best noise performance, however it is not achieved in this design, since increasing size of Mb affects stability. C_{out} is required to be small, and is designed to be the parasitic capacitance at the output node. R is selected as small as possible but large enough to have the output poles much smaller than the input pole. The input pole is defined by the input signal, and is determined through Matlab simulation. The ENC is numerically optimized. For 50 pF input capacitance and 100 nA leakage current, the optimized ENC is around 6700 electrons, which is a better result compared to [3]. Post-layout simulation reveals an ENC level of 8000 electrons. The biasing current in this design is chosen as $1mA$ for the main branch, and $0.5mA$ for the RGC branch. The transistor sizes and their contributions are listed in table I.

C. Design issues

A larger R and a smaller C_{out} is in favored in the preamplifier design. However, large R leads to large voltage

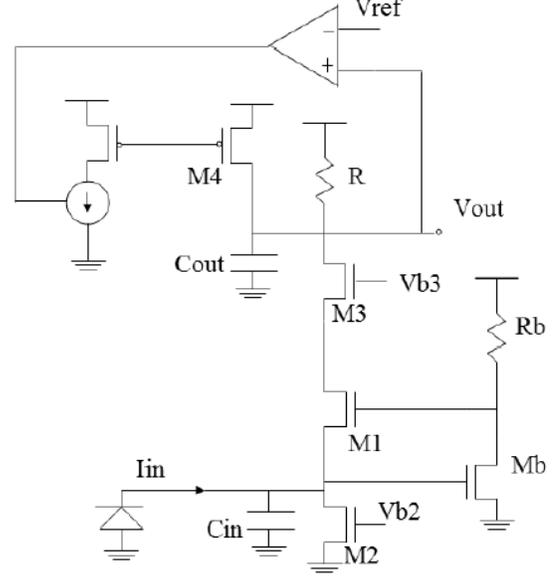| Transistors	W/L ratio	Noise contribution
M1	68	0.003%
Mb	136	82%
M2	40	18%
M3	5.6	0.04%
M4	60	0.06%

Fig. 4. Schematic with added current mirror

headroom, which is directly related with power consumption. An additional current mirror is added in figure 4 to divert part of the biasing current. Also a feedback loop is applied to control the additional current mirror. The feedback loop also makes the preamplifier adaptable to different leakage current. The amplifier in the loop has a very low bandwidth so that it won't effect the output signal.

However, two problems remain. The parasitic capacitance of $M4$ increases C_{out} significantly. Because $M4$ suffers from low mobility and must be quite wide to carry a large current. This issue is combated with another cascode transistor $M3$. With a smaller biasing current, $M3$ can be sized small. Noise analysis shows its noise contribution is negligible.

Another problem is that the added current mirror produces more noise. A comparison between smaller R without additional current mirror and larger R with additional current mirror is provided in [5]. It is derived that the added current mirror has about $\alpha(2\gamma-1)$ times more noise, where $I_{d4} = \alpha I_{d1}$ and γ is the thermal noise factor.

III. SIMULATION RESULTS

The circuit was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models.

Figure 5 shows the simulated transient response. The gain of the preamplifier is about 250 mV/fC. Figure 6 shows
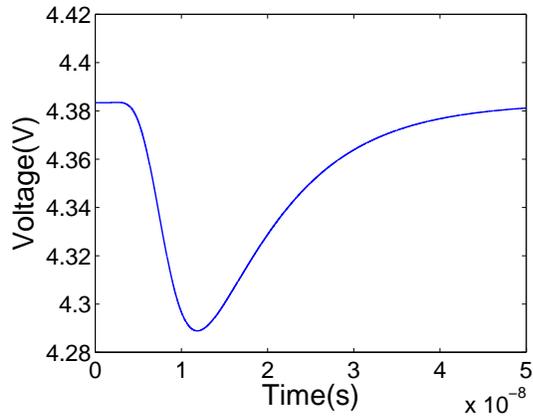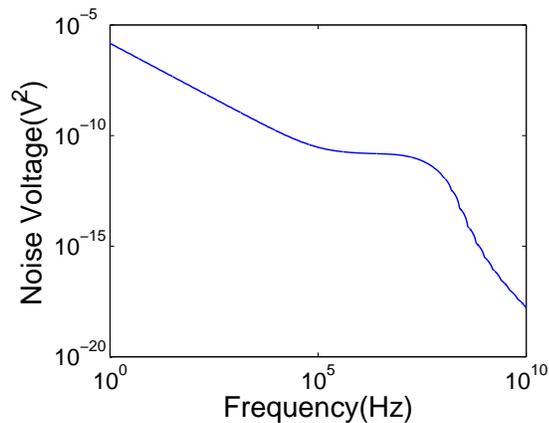
Fig. 5.   Simulated transient response

Fig. 6.   Simulated output noise

Fig. 7.   Core layout of preamplifier

Fig. 8.   Output voltage pulse for input current pulse corresponding to 100,000 electrons

the simulated equivalent output noise. White noise and 1/f noise are dominated in the low frequency range, and the high frequency noise is filtered out at the output pole.

The designed chip was fabricated through 0.5μm CMOS process with 2 poly and 3 metal layers. The chip works with a single 5-V supply and has an overall power consumption of $7mW$. The core layout is shown in figure 7. A preliminary PCB test environment was setup and figure 8 shows a picture of the output signal where the input current pulse corresponds to charge of 100,000 electrons. The input pulse was simulated as a voltage step with $5ns$ rise time passing through a 1 pF capacitor connected serially to the input.

IV. CONCLUSION

In this paper, a current mode regulated cascode preamplifier is designed. It shows several advantages over a common gate structure, especially in applications with large input capacitance. The preliminary prototype of the preamplifier is implemented using 0.5μm CMOS technology and a preliminary test is performed. Its noise performance will be measured in future testing. Design of a proper shaping filter is required to further improve the ENC.
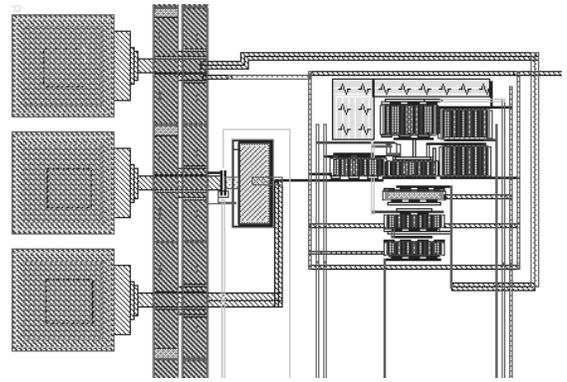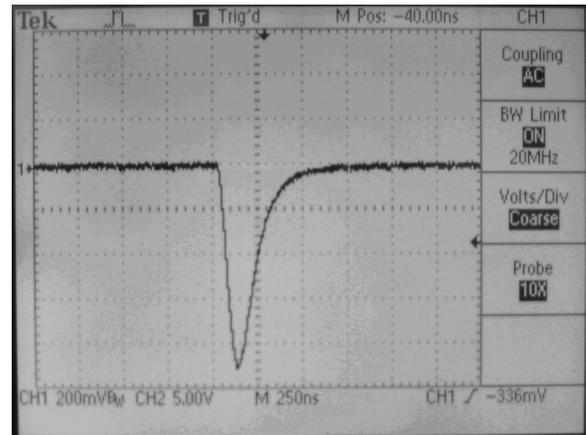
V. ACKNOWLEDGMENTS

REFERENCES

[1] A. Kastalsky, S. Luryi and B. Spivak, "Semiconductor high-energy radiation scintillation detector," Nucl. Instr. Meth. Phys. Res. A 565, pp. 650-656 (2006).
[2] T. Noulis, C. Deradonis, and S. Siskos, "Advanced Readout System IC Current Mode Semi-Gaussian Shapers Using CCIIs and OTAs," VLSI Design, Vol. 2007, Artical ID 71684.
[3] F. Anghinolfi, P. Jarron, F. Krummenacher, E. Usenko and M.C.S.Williams, "NINO: An Ultrafast Low-Power Front-End Amplifier Discriminator for the Time-of-Flight Detector in the ALICE Experiment," IEEE Tran. on Nuclear Science, Vol. 51, No. 5, Oct. 2004.
[4] S. M. Park, H. Yoo, "1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications," IEEE J. Solid-State Circuits, Vol. 39, No. 1, Jan. 2004.
[5] Behzad Razavi, "Design of Integrated Circuits for Optical Communications," McGraw Hill press, 2003.