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Microwave performance of top-collector charge injection transistors on InP substrates

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Abstract. Charge injection transistors have been implemented in molecular beam epitaxy grown InGaAs/InAlAs/InGaAs and InGaAs/InP/InGaAs heterostructures using a self-aligned process for the collector stripe definition. Scattering parameters have been measured in the frequency range from 100 MHz to 40 GHz. InP barrier devices show the best microwave performance ever reported for a real-space transfer transistor: at 40 GHz the short circuit current gain $|h_{21}|$ is 8 dB and the power gain is larger than unity. The slope of $|h_{21}(f)|$ depends on the bias point and is generally gentler than 20 dB decade^{-1}. Extrapolating at the measured slope, we find $|h_{21}| = 1$ at $f = 115$ GHz. The short circuit current gain cut-off f_T, defined by extrapolation at 20 dB decade^{-1} from the point of least mean square deviation of the measured slope from 20 dB decade^{-1}, is $f_T = 73$ GHz. Devices with InAlAs barriers show a relatively slower performance ($f_T = 32$ GHz). The difference is discussed in terms of the relative rates of intervalley scattering and real-space transfer in the two heterostructures.

1. Introduction

The charge injection transistor [1] or CHINT is a three-terminal heterojunction device based on the real-space transfer (RST) of hot electrons between two conducting layers. The heating electric field along the *emitter* channel, which plays the role of a hot-electron cathode, is provided by the voltage between '*source*' and '*drain*' electrodes. The other, '*collector*', layer is separated from the emitter by a heterojunction barrier and is contacted separately.

Microwave properties of CHINTs have been studied experimentally [2–5] in several material systems (GaAs/AlGaAs [2], InGaAs/InAlAs [3], strained-layer InGaAs/AlGaAs/GaAs [4, 5]) and theoretically using Monte Carlo (MC) simulations [6–8]. The ultimate frequency performance of the device is believed to be limited by the time of flight of hot electrons over high-field regions of the device, i.e. over distances of the order of the barrier layer thickness. A recent experimental study [5], subsequently supported by MC simulations [7], showed that the intrinsic f_T of a CHINT with a collector width of $L_{CH} \approx 1$ μm is about three times higher than that of an FET with the same gate width.

Previously reported high-speed RST transistors have been implemented in either collector-down [2, 3] or collector-up [4, 5] configurations. Collector-down devices have an unavoidable overlap between the source/drain regions and the collector layer which gives rise to parasitic capacitances and limits the microwave performance. The best reported f_T in a collector-down CHINT was 40 GHz (with the maximum available gain MAG > 1 at the highest measured frequency of 25 GHz) obtained in a InGaA/InAlAs heterostructure with a 2000 Å thick InAlAs barrier [3]. Collector-up configurations offer significant advantages in that the parasitic capacitances can be effectively eliminated by patterning the collector stripe. The highest reported frequencies in a collector-up CHINT [4] were $f_T = 60$ GHz (obtained by extrapolating the data measured up to 25 GHz) and a lower $f_{max} = 18$ GHz (presumably due to parasitic resistances in a non-self-aligned structure).

This is the first report of the microwave performance of a self-aligned top-collector CHINT, implemented in MBE-grown heterostructures, lattice-matched to InP. Our self-aligned process has been previously used in the implementation of a complementary light-emitting CHINT [9]. We have studied both InAlAs and InP barrier devices. The use of an InP barrier is reported for the first time in a unipolar CHINT; these devices also show the best microwave performance ever reported for an RST transistor.

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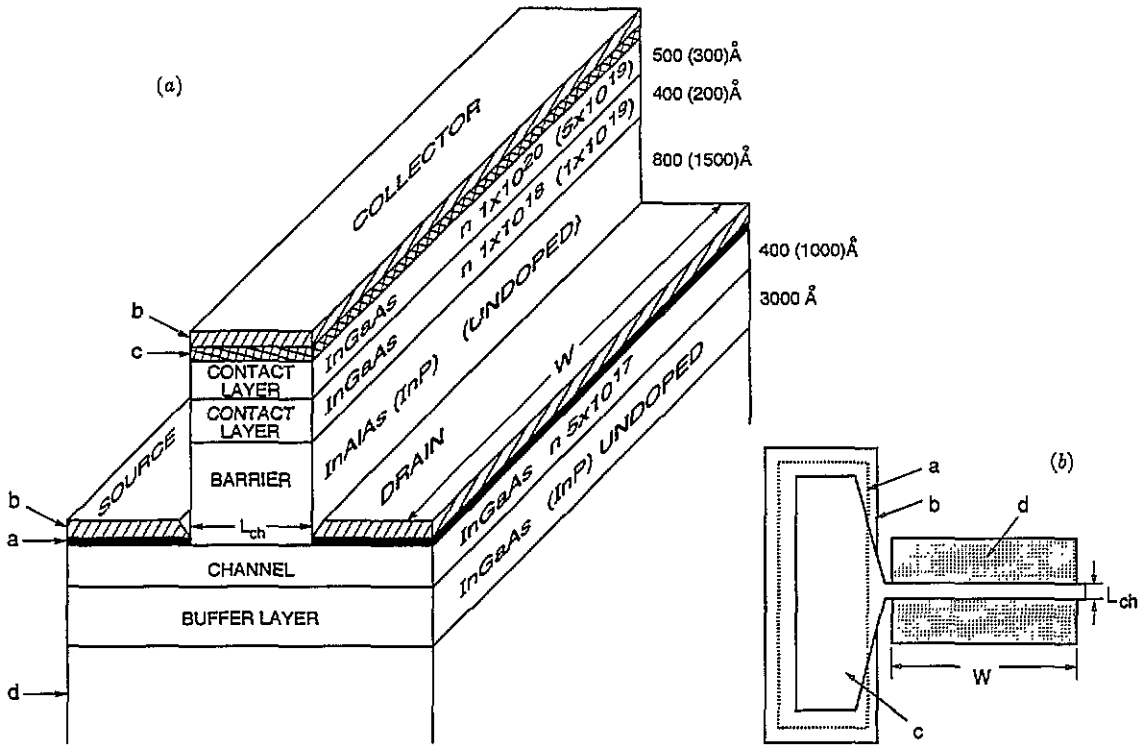

Figure 1. Structure and layout of collector-up microwave charge injection transistors. In the cross-sectional view (*a*) the letters and numbers in parentheses refer to the InP barrier device: a, 450 Å Ni/Ge/Au/Ag/Au alloyed channel contact; b 3000 Å Si_3N_4 layer; c, 2000 Å Au collector contact; d, semi-insulating InP substrate. In the layout (*b*) the indicated levels are: a, the pit; b, the Si_3N_4 patch; c, the collector; d, the source/drain contacts.

2. Device fabrication

The $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterostructure was grown by molecular beam epitaxy (MBE) and the $In_{0.53}Ga_{0.47}As/InP/In_{0.53}Ga_{0.47}As$ by metallorganic MBE (MOMBE). Details of the growth and processing have been described elsewhere [9]. Devices were fabricated using standard optical lithography and selective wet etching. The device structure is illustrated in figures 1(*a*) and 1(*b*).

Figure 1(*b*) shows the mask layout for microwave transistors. The spatula-shaped central feature is the collector metal. Our first step was to etch down to the buffer layer (cf figure 1(*a*)) in a rectangular 'pit' area (a) covering the wide part of the future spatula. The purpose of this step was to eliminate the channel under the wide part of the collector in order to minimize the parasitic capacitance from the RST-inactive area. Next, the pit was covered by a silicon nitride patch over a slightly wider rectangular area (b). The narrowest separation between the edges of the pit and the patch was 1.5 μm. Subsequently 2000 Å thick Au layer was patterned (by lift-off) into the spatula shape (c) of the collector. This layer was then used as a mask for etching the structure down to the channel layer.

The etching procedure was different for devices with different barriers. For an InAlAs barrier we used a non-selective phosphoric acid-based solvent to rapidly etch down to approximately the middle of the barrier and then used HCl/H_2O (2:1) to etch the remaining portion of the barrier selectively, stopping at the InGaAs channel layer (figure 1(*a*)). For an InP barrier we first selectively removed InGaAs layers and then selectively etched the InP layer by HCl/H_2O (1:1).

A key processing step involves evaporation of self-aligned source/drain metal (d) which has to provide ohmic contacts to the channel without degrading the integrity of the barrier. The contacts were evaporated using a standard Ni/Ge/Au/Ag/Au sequence—but the total thickness was only 550 Å—and alloyed at 300 °C for 5–15 s. In the last stage of the fabrication both wafers were blanket covered with a 3000 Å thick Si_3N_4 layer deposited at 300 °C, windows were opened and final metal (Ti/Au, 3000 Å) was evaporated to form contact pads.

Devices reported in this work had $L_{CH} \times W = 1 \times 20$ μm^2. The separation between the edges of b and d is 2 μm and the breakpoint of the spatula c is in the middle between the edges of b and d. Our use of relatively heavy doping in the emitter channel (5×10^{17} cm^{-3}) has resulted in a high yield and reproducibility, as well as a higher RST current prior to the onset of instabilities associated with NDR in the channel.

3. Experimental results

Figures 2(*a*) and 2(*b*) show the static characteristics of the InP barrier and InAlAs barrier devices respectively. InP barrier devices show higher output current (I_C) at

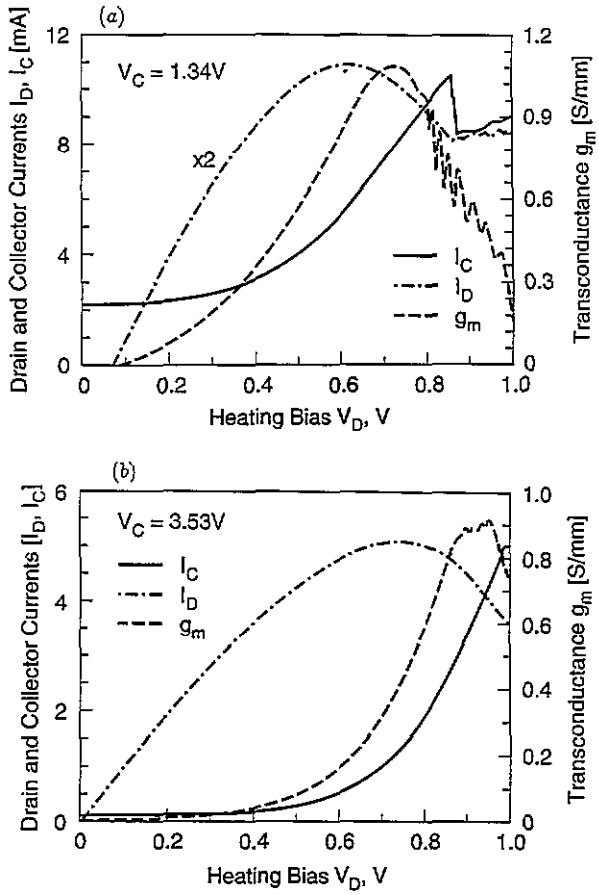

Figure 2. Room-temperature characteristics of a collector-up CHINT at a constant collector bias V_C: (*a*) InP barrier, (*b*) InAlAs barrier.

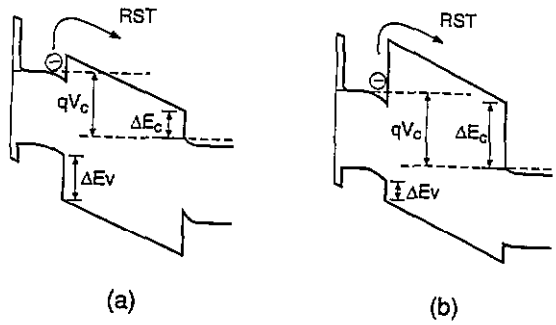

Figure 3. Band diagram of a device cross section near the source under a positive bias applied to the collector: (*a*) the $In_{0.53}Ga_{0.47}As/InP/In_{0.53}Ga_{0.47}As$ heterostructure, (*b*) the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterostructure.

lower values of the heating and collector biases (V_D, V_C). This is explained by the lower conduction band discontinuity; $\Delta E_C = 0.25$ eV in the $In_{0.53}Ga_{0.47}As/InP$ heterojunction compared with $\Delta E_C = 0.5$ eV in the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunction [10] (cf figure 3), which leads to the lower RST threshold in InP barrier devices. At the same time, the leakage current of cold carriers (in the absence of an RST) is also higher in these devices. The transconductance $g_m = W^{-1}\partial I_C/\partial V_D$ has a similar behaviour in the two devices (cf figure 2). In the range of biases investigated the maximum value of g_m is 1.1 S mm^{-1} for InP barrier devices and 0.9 S mm^{-1} for InAlAs barrier devices.

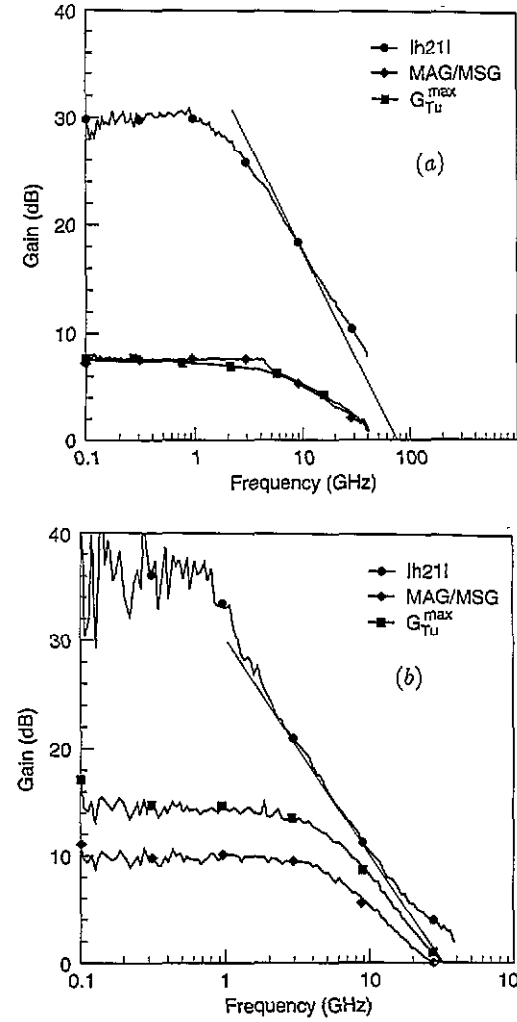

Figure 4. Small-signal gain parameters at room temperature, calculated from the measured S-parameters at the following DC bias configurations: (*a*) InP barrier devices, $V_C = 1.34$ V, $V_D = 0.61$ V; (*b*) InAlAs barrier device, $V_C = 3.53$ V, $V_D = 0.75$ V. The selected bias voltages (V_C, V_D) correspond to the maximum quasi-static gain of the device, measured at 100 MHz. Full lines correspond to the extrapolation at −20 dB decade^{-1}.

We characterized the high-frequency operation of CHINTs using a vector network analyser. The device being studied was operated in the common-source configuration with the input signal applied to the drain and the output taken from the collector. Scattering parameters were measured on-wafer in the range from 100 MHz to 40 GHz. Pad parasitics were removed by subtracting the Y-parameters of a pad without a device from the Y-parameters of the measured device. The frequency dependence of the magnitude of short-circuit current gain $|h_{21}|$, the power gain MAG/MSG, and the unilateral gain G_{Tu}^{max} are shown in figure 4. MAG is plotted when the stability factor $K > 1$; MSG (the maximum stable gain) is plotted for $K < 1$.

For InP barrier devices (figure 4(*a*)) we found $f_T = 73$ GHz, obtained by extrapolating the data at −20 dB decade^{-1} through the point of least deviation of the measured slope from −20 dB decade^{-1}. This gives a very conservative estimate: the actual slope is only −16.5 dB decade^{-1} and extrapolating the curve at this

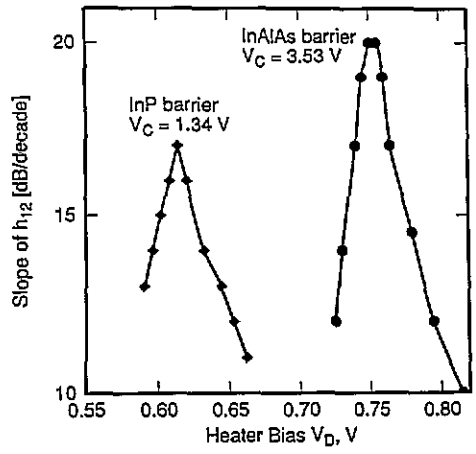

Figure 5. Variation of the high-frequency slope $\partial|h_{21}|/\partial f$, measured at the point of its least deviation from −20 dB decade^{-1}, with the heating bias V_D at a constant collector bias V_C.

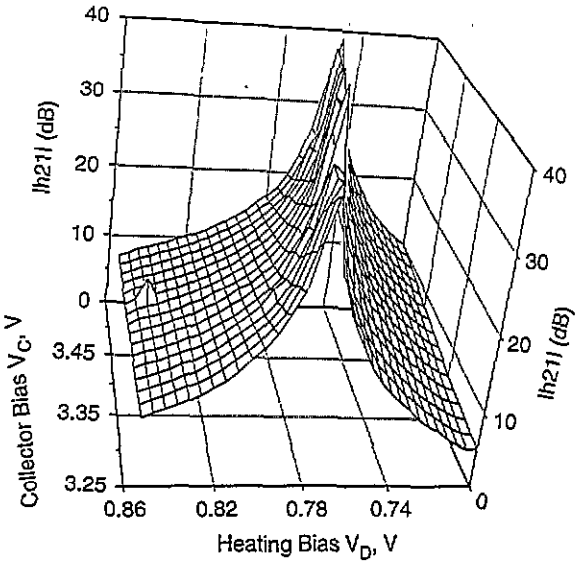

Figure 6. Dependence of the quasi-static (f = 700 MHz) short-circuit current gain $|h_{21}|$ on the DC bias conditions for the InAlAs barrier device.

slope would give a cut-off of 115 GHz. At 40 GHz the measured $|h_{21}| = 8$ dB and the power gain is larger than unity. In InAlAs barrier devices (figure 4(*b*)) the extrapolation at the steepest slope (which is actually −20 dB decade^{-1}) gives $f_T = f_{max} = 32$ GHz; it should be noted, however, that at 40 GHz the measured $|h_{21}|$ is still > 1.

The slope of $|h_{21}(f)|$ is an extremely sensitive function of V_D. The nature of this dependence is not understood. In contrast, the dependence of the slope on V_C is relatively weak. Figure 5 shows the variation of the slope $\partial|h_{21}|/\partial f$ in both devices at fixed values of V_C (corresponding to the data plotted in figures 4). It is not clear why the peak slope is higher in InAlAs barrier devices.

Quasi-static characteristics of the device also strongly depend on the heating bias V_D and weakly on the collector bias V_C. A three-dimensional plot of $|h_{21}(V_D, V_C)|$ measured at 700 MHz is presented in figure 6 for the InAlAs barrier (the InP barrier is similar). A variation in V_D as small as 10 mV near the DC current gain maximum changes $|h_{21}|$ by more than 10 dB within the entire quasi-static band of about 1 GHz. This extreme sensitivity of $|h_{21}|$ to quasi-static DC bias may find useful applications. At the same time, the f_T changes little if at all, because the slope of $|h_{21}(f)|$ peaks sharply at the same V_D (cf figure 5).

4. Discussion

We have found that InP barrier devices show f_T more than twice that of devices with an InAlAs barrier, fabricated using the same mask set and a virtually identical process. It should be further noted that the barrier thickness in our InP barrier devices was chosen to be twice that of the InAlAs barrier. This was done to diminish the parasitic leakage of cold carriers at zero drain bias in InP barrier devices (cf figure 2). Thus, we find the surprising result that InP barrier devices are faster than InAlAs barrier devices, even though the latter have a barrier only half as wide and far more ideal (from the leakage standpoint) static characteristics. Let us discuss the possible origin of this significant difference in performance.

One of the fundamental speed limits in a CHINT is due to the finite time of flight of electrons across the barrier. In order to ascribe our present results to this limitation, one would have to assume that the average velocity of carriers in InAlAs barrier is more than four times slower than that in InP barrier. This assumption does not seem to be plausible if we compare the generally accepted [11] values of peak and saturation velocities in InAlAs (1.8×10^7, 4×10^6 cm s^{-1}) and InP (2.3×10^7, 1×10^7 cm s^{-1}). The possibility of a non-equilibrium transport effect (like overshoot) favouring InP does not appear likely, since at the bias configuration of our microwave measurements the electric field across the barrier has been much larger in InAlAs devices. Thus, the difference in the barrier widths is not likely to be the cause of the different microwave performance.

Had we been dealing with conventional collector-down transistors [3, 4], we would naturally explain the slower microwave performance of InAlAs devices in terms of the higher parasitic drain–collector capacitance in devices with narrower barriers. However, it is the central idea motivating the development of collector-up devices that the drain–collector capacitance no longer has a significant extrinsic component (i.e. that due to the contact area outside the channel) and the effect of the intrinsic drain–channel capacitance reduces to the time of flight of RST carriers across the barrier [1–8]. Although without a systematic study of the microwave characteristics of collector-up CHINTs implemented in the same material system with different barrier widths we cannot dismiss the possibility of a parasitic capacitance effect, the difference in the barrier widths does not seem to be the likely cause of the slower microwave performance of InAlAs barrier devices.

We believe that the different microwave performance may be explained by intervalley scattering effects manifesting themselves differently in the two materials, due to the difference in their heterojunction line-ups (figure 3). Indeed, the satellite valley separation in InGaAs ($E_{\Gamma L} = 0.55$ eV [12]), which determines the threshold for intervalley scattering, is comparable in InAlAs barrier devices with the conduction band discontinuity $\Delta E_C \doteq 0.5$ eV [10], which determines the RST threshold. This means that a large fraction of hot electrons in InGaAs with energies above ΔE_C actually reside in L valleys. These electrons cannot go across the barrier because the L valley position in InAlAs is still much higher ($E_{\Gamma L} = 0.35$ eV [11]). Therefore, the RST in InGaAs/InAlAs depends on the establishment of a hot-electron equilibrium between Γ and L valleys and may be substantially slowed down by this process. This interpretation is in agreement with the discussion by Kizillyalli and Hess [6]. In contrast, in InP barrier devices, where the RST threshold is substantially lower, $\Delta E_C = 0.25$ eV $\approx 0.5 E_{\Gamma L}$ (InGaAs), intervalley scattering is not likely to be important.

Acknowledgments

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