Multi-emitter Si/Ge_xSi_{1-x} Heterojunction Bipolar Transistor with No Base Contact and Enhanced Logic Functionality

A. Zaslavsky, S. Luryi, C. A. King, and R. W. Johnson

***Abstract*—We demonstrate multi-emitter Si/Ge_xSi_{1-x} npn heterojunction bipolar transistors (HBT's) which require no base contact for transistor operation. The base current is supplied by the additional emitter contact under reverse bias due to the heavy doping of the emitter-base junction. Large-area HBT test structures exhibit good transistor characteristics, with current gain $\beta \approx 400$ regardless of whether the base current is supplied by a test base electrode or one of the emitter contacts. These devices have enhanced logic functionality because of emitter contact symmetry. Since device fabrication does not require base electrode formation, the number of processing steps can be reduced without significant penalty to HBT performance.**

I. Introduction

As microelectronic circuits progress toward greater integration and ever smaller feature sizes, increasing the logic functionality and decreasing fabrication complexity is becoming a primary direction in semiconductor device research. Higher logic functionality has been demonstrated in multiterminal real-space transfer [1]–[3] and resonant tunneling [4], [5] heterostructrues, but usually at the cost of effective integration with mainstream technology. In this letter, we demonstrate an enhanced functionality double-emitter npn heterojunction bipolar transistor (HBT) fabricated in the Si/Ge_xSi_{1-x} material system, [6] which retains the advantageous properties of Si/GeSi heterojunctions for high-performance HBT's, [7] as well as compatibility with silicon technology. In our devices, the emitter-base junction is doped heavily and two emitter contacts are fabricated, while the base is left floating. The emitter-base diode $I(V)$ characteristic allows emitter contacts to extract the base majority carriers under reverse bias, so the emitter contacts can perform either emitter or base electrode functions [6], [8]. Our npn HBT's exhibit good transistor characteristics, with current gain $\beta \approx 400$ in large-area devices, when either of the emitter contacts serves as the base electrode. Finally, we note that since these HBT's require no base contact, they are well-suited for BiCMOS circuits, where the simplified bipolar fabrication will help integration with standard CMOS designs.

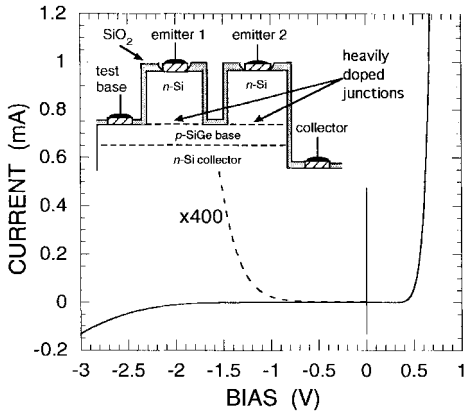

Fig. 1. Diode characteristic of the Si/$Ge_{0.2}Si_{0.8}$ emitter-base junction. Dashed line is the inverted reverse bias characteristic multiplied by the common-emitter current gain ($\times 400$), useful for predicting the transconductance in the multi-emitter HBT in the floating-base mode. Inset shows the four-terminal HBT test structure, which permits a comparison of transistor characteristics in the standard (base current I_B supplied by the base electrode) and floating-base (I_B supplied by the second emitter in reverse bias) modes, as well as emitter-base diode characterization.

II. Experimental

Wafers of Si/$Ge_{0.2}Si_{0.8}$/Si npn HBT material were grown by rapid thermal chemical vapor deposition [9] on n^+-Si substrates, with the following structural parameters: a 1.1-μm thick n-Si subcollector region doped 4×10^{17} cm^{-3}, a 300 Å p^+-$Ge_{0.2}Si_{0.8}$ base doped 4×10^{19} cm^{-3} except for unintentionally doped 40 Å spacers on both sides, and a 0.2-μm thick n^+-Si emitter layer doped 2.8×10^{18} cm^{-3}. We fabricated large-area double-emitter HBT test structures, illustrated in the inset of Fig. 1, as follows: large (100×100 μm) emitter areas were protected with deposited SiO_2; selective wet chemical etching down to the base layer was achieved with an isopropanol-KOH solution that stops at the p^+-GeSi base [10]; Au/Pt base metal contact evaporation was followed by etching through the base layer in a CF_4 plasma with the emitter-base region protected by a photoresist mask; finally, Al emitter contact metal was evaporated. The sidewalls were passivated with deposited SiO_2 and the emitter-base and emitter-emitter trench separations were lithographically

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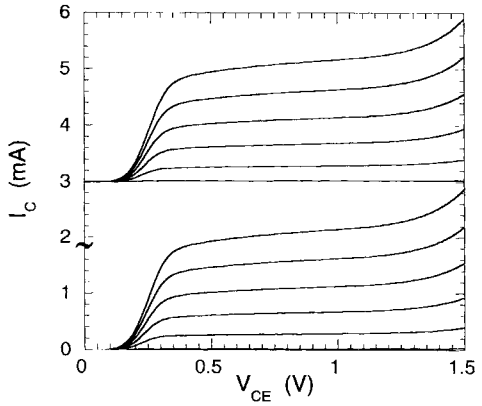

Fig. 2. Comparison of transistor $I_C(V_{\rm CE})$ characteristics of the Si/$Ge_{0.2}Si_{0.8}$/Si HBT test structure in the standard (top) and floating base (bottom) modes. In both cases $I_B = 0$–5 μA, in 1 μA increments.

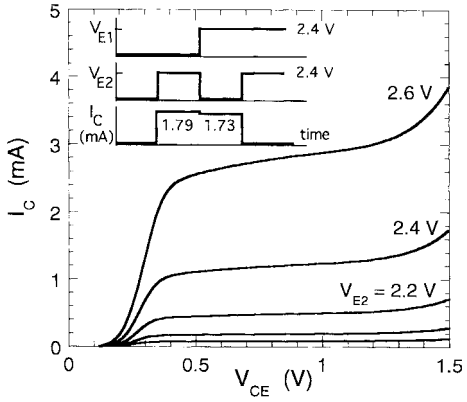

Fig. 3. Transistor $I_C(V_{\rm CE})$ characteristics of a Si/$Ge_{0.2}Si_{0.8}$/Si double-emitter HBT with no base contact and oxide-passivated surfaces as a function of the voltage difference between the two emitters: $V_{E1} = 0$ (grounded), $V_{E2} = 1.82.6$ V, in 0.2 V increments. If the emitter biasing is interchanged, $I_C(V_{\rm CE})$ remains the same. The transconductance $I_C(V_{E2})$ can be graphically obtained from emitter-base junction diode characteristic in Fig. 1: for a given value of I_C, the required V_{E2} is the horizontal distance between the forward bias and rescaled (multiplied by $-\beta$) reverse bias curves (dashed line in Fig. 1). Inset shows the exclusive or functionality of a single device: $I_C = {\rm XOR}(V_{E1}, V_{E2})$, where V_{E1}, V_{E2}, and a fixed collector bias $V_C = 1.5$ V are relative to ground. In the two off-states the output current is negligible, $I_C < 0.01$ mA.

defined to be several microns (see Fig. 1 inset). The electrical characteristics were probed at dc using a parameter analyzer. The inclusion of a test base electrode in these structures made it possible to compare the floating-base double-emitter HBT (where one of the emitters provides the base current under reverse bias) to conventional HBT performance, as well as measure separately the emitter-base diode $I(V)$ characteristic. Subsequently, double-emitter HBT's with no base contact and SiO_2 sidewall passivation were fabricated by analogous means.

III. Results and Discussion

The room temperature $I(V)$ of the Si/$Ge_{0.2}Si_{0.8}$ emitter-base junction is shown in Fig. 1. Heavy emitter-base junction doping leads to the intentionally rapid reverse-bias breakdown, with the current rising to the μA range for $V_{\rm EB} \leq -1.5$ V.

A comparison of the transistor characteristics of the Si/$Ge_{0.2}Si_{0.8}$/Si structure in the standard and floating-base modes is shown in Fig. 2. The top $I_C(V_{\rm CE})$ characteristic corresponds to either of the emitter contacts serving as the emitter electrode (the other is left floating), and the base current $I_B = 0-5$ μA supplied via the test base electrode. The common-emitter current gain $\beta \approx 400$, which is reasonable for our HBT parameters. The bottom $I_C(V_{\rm CE})$ characteristic in Fig. 2 corresponds to the same device in floating-base mode: one of the emitter contacts serves as the emitter electrode, the other emitter contact supplies the base current, while the test base contact floats. The transistor characteristics are preserved, including the current gain. Clearly, a conventional ohmic base contact is not necessary to achieve transistor amplification in such a device, because a reverse-biased emitter-base junction serves as a contact to the base layer. The efficiency of this base contact depends on the emitter-base $I(V)$ characteristic and can be improved by increasing the emitter and base doping to high 10^{18} cm^{-3} and high 10^{19} cm^{-3} ranges, respectively—the resulting backward-diode junction should pass current at even small reverse bias values [11]. Since contact formation to narrow HBT bases is a technologically difficult procedure, the simultaneous fabrication of emitter contacts with both emitter and base electrode functionality leads to considerable processing simplification.

In addition to the fabrication advantages of multi-emitter HBT's with no base contact, these structures offer enhanced logic functionality due to emitter contact symmetry. Consider the transistor characteristics of a double-emitter device as a function of the voltages on the two emitters, V_{E1} and V_{E2}. If both of the emitter contacts are grounded $(V_{E1} = V_{E2} = 0)$ and the collector is biased high $(V_C \gg kT)$, a negligibly small collector current will flow as in a standard bipolar transistor with a floating base. Conversely, if one of the emitter contacts is grounded $(V_{E1} = 0)$ and the other is at some sufficiently large positive bias V_{E2}, the reverse-biased emitter-base junction under the second emitter will provide an appreciable base current, leading to a large output current I_C. This is illustrated in Fig. 3, which shows the operation of a double-emitter HBT with no base electrode and SiO_2 passivated sidewalls. The collector current $I_C(V_{\rm CE})$ with $V_{E1} = 0$ (first emitter contact grounded) is shown as a function of V_{E2} (stepped in the 1.8–2.6 V range). In this active transistor mode with high common-emitter current gain β, the forward-biased first emitter current density I_1 is related to the reverse-biased second emitter current density I_2 by

$$I_C \approx I_1 = \beta I_2 \tag{1}$$

as long as we ignore junction leakage. The transconductance $I_C(V_{E2})$ can then be predicted by graphical construction from the emitter-base diode characteristic shown in Fig. 1 [11]. Bu inverting the reverse bias emitter-base diode $I(V)$ and multiplying by β (dashed line in Fig. 1), one can read off the biasing difference (V_{E2}–V_{E1}) between the emitter contacts for a given collector current I_C as the horizontal (voltage) distance between the forward bias curve and the rescaled reverse bias curve. Thus, Fig. 1 would predict $I_C \approx 0$ for $V_{E2} < 1.6$ V, because below 1.6 V the reverse-biased emitter-base current is

negligible, and $I_C = 1.2$ mA for $V_{E2} \approx 2.4$ V, in agreement with Fig. 3.

Since the emitter contacts are fully symmetric, double-emitter devices possess full exclusive or logic functionality, illustrated schematically in the inset of Fig. 3. By fabricating more than two contacts to the emitter region, more complicated logic functions can be implemented. For example, an analogous three-emitter contact structure can perform the ornand logic function in a single device [6], [8]. It should be noted that the logic functionality of multi-emitter HBT's does not require their implementation in the Si/GeSi material system and, in fact, the ornand logic function of a three-emitter structure has already been demonstrated in a III–V multi-emitter HBT [8]. However, we believe the principal application of these devices will come in BiCMOS circuitry, where high-current drive bipolar transistors are integrated with silicon CMOS logic. In this regard, our Si/GeSi implementation of the higher-functionality multi-emitter HBT with no base contact and simplified processing is highly advantageous compared to the compound semiconductor version [8]. Furthermore, the structural parameters of our devices are consistent with high-performance npn Si/GeSi/Si HBT's: since the Si/Ge_xSi_{1-x} band discontinuity occurs almost entirely in the valence band ($\Delta E_V \approx 0.16$ in $Si/Ge_{0.2}Si_{0.8}$), [12] very high base doping can be achieved without sacrificing emitter efficiency. The same heavy doping reduces the resistance of the reverse-biased emitter-base diode—if the emitter and base were doped high 10^{18} cm^{-3} and high 10^{19} cm^{-3}, respectively, a low reverse-bias resistance would result. The ultimate achievable base contact resistance is difficult to predict without a quantitative backward-diode model applicable to Si/GeSi heterostructures, but our preliminary estimates show that the penalty in speed compared to standard Si/GeSi HBT's would not be too large. At the same time, optimized multi-emitter HBT's promise the above-described advantages in logic functionality and reduced fabrication complexity.

IV. Conclusions

We have implemented the first multi-emitter npn Si/GeSi HBT structures and confirmed their transistor operation in the floating-base mode, including high gain and enhanced logic functionality. These devices are advantageous from the processing viewpoint since they do not require a base contact, which is a demanding step in HBT fabrication, and are fully compatible with silicon technology. Their additional logic functionality is due to the emitter contact symmetry: the fact that either of the emitter contacts can provide a base current makes it possible to implement an exclusive or gate in a single device. This makes them promising for BiCMOS circuits, such as CMOS logic integrated with high current-drive bipolar Si/GeSi input-output devices.

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