ON FUTURE ORGANIZATION OF HYBRID CHIP MANUFACTURING

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Abstract

According to a number of forecasts, the microelectronics industry is at the threshold of revolutionary changes. One of the anticipated changes is the future transition to a high-volume production of hybrid chip systems. In this paper we consider issues associated with the manufacturing organization of such systems. A simple cost-volume model developed in this work identifies economic conditions that will drive the organizational paradigm shift to provide both the higher profit to the new organizational form and a high entry barrier to the competition.

1. Introduction: Some Trends in VSLI Industry

There are numerous indications that we are at a turning point in the evolution of the giant VLSI industry. For many years the celebrated silicon technology has known a virtually one-dimensional path of development: reducing the minimal size of lithographic features. There is now widespread recognition that this path has brought us to the point of diminishing return. The often quoted Moore's Law – supposed to express the exponential nature of the VLSI progress – is in fact slowing down (see, e.g., Brenner 1997). In 1965 when Intel's founder Gordon Moore proclaimed his exponential law, the time constant in that exponent – corresponding to the doubling of the number of transistors on a manufactured chip – was once every 12 months. That would be growing by a factor of 1000 every decade. By the mid 1970's when Moore's Law was firmly entrenched, the actual time constant was about 18 months – and this corresponds to a factor of about 100 every decade. By the end of 1980's this was no longer valid and the actual time constant was about 2 years. The 1994 SIA Road Map assumes a growth of only about factor of 10 between 1997 and 2007 for microprocessors, implying a time constant of 3 years (to be sure, this projection is likely to be further adjusted).

Realization of this hard reality by captains of the industry has led to a noticeable shift of investment from new technologies to software and circuit design within existing technologies. There is certainly no shortage of opinion about these trends. Some, haunted by the specter of the steel industry, believe that the semiconductor industry has matured and the research game is over. Others believe the progress in hardware technology will come back roaring, based on innovative research. We certainly belong to the latter category. However, the innovative research that we anticipate will be markedly different from that we have been witnessing over the past 20-30 years. Instead of shrinking the dimensions of Si devices, or perfecting exotic compound semiconductor technologies, successful researchers will broker marriages between these technologies. There is no doubt that silicon will remain the dominant semiconductor material; teaching new trick to the old dog will be the key to success. In this context, we believe that most significant applications of compound semiconductor electronics will be associated with its use in silicon electronics.

With the above considerations in mind, we focus our consideration on the integration of high-performance electronic and optoelectronic devices and small systems with Si circuits, based on advanced packaging concepts and interconnect technology. It is our vision that future electronic systems will have critical needs in on-chip transformation of the signal power among electrical, optical, and microwave media. Communication between relatively small subsystems on the same chip and interchip communications from chip interior will enable qualitatively new systems.

This point of view has been a common theme echoed by a number of panelists at this FTM conference "Off the Beaten Path" (June, 1998) and at the earlier FTM meeting "Reflections on the Road to Nanotechnology" (France, July 1995). It has been endorsed by other think tanks as well. The US Army Electronics Strategy Planning Workshop (January, 1995) has identified as "Extremely High Priority" the research thrust in Advanced Electronic and Optoelectronic Materials with the following justification:

> "It is anticipated that future Si IC technology will evolve to incorporate ultra-high performance electronic and opto-electronic on-chip elements. These elements will facilitate input-output functions from the chip interior, as well as high-bandwidth intrachip communication. Relatively small Si subsystems (less than 100,000 gates) need to be internally interconnected using minimum-feature rules. To achieve these goals, research needs to be directed toward: (1) advanced packaging concepts; (2) hybrid devices based on mixed compound semiconductor structures on Si; (3) novel device concepts relating to mixed materials architectures; (4) novel very large scale integrated circuit architectures that take advantage of the wide-band communication between parallel subsystems on a Si chip."

The logic of industrial evolution will motivate new paths for a qualitative improvement of system components, other than the traditional path of a steady reduction in fine-line feature size. It is widely accepted that some, perhaps most of the future systems will be on-chip systems with

inclusion of foreign elements (e.g. compound semiconductor) into CMOS chips. It will be done by using special islands, interconnected with the rest of the chip via final metal lines (Kaloyeros et al., 1997). This incorporation is done on a whole wafer scale before dicing the wafer into small chips. Foreign elements included may perform functions otherwise inaccessible to silicone, like e.g. emission or efficient absorption of light, or it may include ultra high performance operations above the capability of SI technology.

One of the promising hybrid technologies is *active packaging* (Luryi, 1996) which is a device fabrication technique, intended to implement devices on a foreign platform that perform better than conventionally fabricated devices on their natural semiconductor substrates. In active packaging certain essential fabrication steps (lithography, etching, metallization, etc.) are performed *after* the partially processed device or circuit is packaged onto a host platform. This often enables the implementation of structures that cannot be realistically obtained in another way, such as those requiring lithography on *opposite* sides of a thin semiconductor film.

One of the most important goals of active packaging is the combination of dissimilar materials (notably, III-V compound semiconductors) with silicon integrated circuitry (IC) on a single Si substrate; Luryi and Sze (1984, 1988). This goal is now widely recognized as an important research direction in microelectronics and is shared by other emerging technologies, such as those based on *heteroepitaxial* and *thin-film transfer* techniques; Doboeck and Borghs (1993).

The hybrid chip technology is not intended to replace conventional devices, but rather to complement them. Hybrid devices are in a sense "discrete" as their number on the chip will be relatively small compared to that of ULSI/TSI transistors. However, development of hybrid chips will offer much higher system performance and broader functions. This technology is compatible with and extends the current "miniaturization" trend in microelectronics as expressed by the celebrated Moore's Law. Whether or not the microelectronics industry will follow Moore's law in the next decade, hybrid chips will become an important step in future developments.

2. Structure of Production Facilities for Hybrid Chips

The paradigm shift to on-chip integrated hybrid system calls for a radical rethinking of the entire manufacturing process – not only at an individual factory level, but at an even deeper level involving dynamic interaction of distinct factories.

Implementation of hybrid technologies may be summarized in the following four steps:

(a) standard VLSI processing of a silicon wafer;

(b) special purpose islands are left virgin on Si wafer or perhaps pits etched in to receive foreign elements;

(c) foreign elements (possibly prefabricated at least partially) are attached to the surface of Si wafer at the sites of specially grown islands;

(d) post-packaging processing, at the minimum including interconnect by final metallization.

The key question addressed in this work is how should such a production be organized ? We shall try to answer this question leaving aside the obvious motivation to perform steps (a) and (b) in different physical locations to avoid contamination. That is not a very strong argument because one technological process can be organized in multiple locations in a multi-echelon production process.

The first basic question is *whether foreign semiconductor incorporation should be included into the Si CMOS process* or separate facilities for steps (c) and (d) should be established?

We believe several arguments are in favor of the second option. This implies coexistence of two kind of factories: one large and steady Si CMOS processing and fabrication facility (referred to below as the *"Foundry"*) the other being a multiplicity of relatively small and entrepreneurial compound semiconductor fabrication and hybrid packaging facilities (*"Hybrid Packagers"*). These arguments include:

(i) Foundry uses a stable and mature technology; introduces changes slowly; uses extremely expensive equipment and facilities; is open to orders from outside via well defined process specifications. Because of the economy of scale, steps (a) and (b) are much cheaper when carried out in this environment.

(ii) Several entrepreneurial Hybrid Packagers provide a pool of orders to the Foundry, thus making the flow of orders more steady, which leads to higher utilization of the Foundry facilities. The effect of pooling is well-known in stochastic models; Wolff (1989).

(iii) The product differentiation is effectively delayed past the Foundry. This makes the Foundry more cost efficient in managing its resources and inventories; see Lee and Tang (1997).

(iv) The "Hybrid Packager" is a high-risk venture, often operating *ad hoc* to produce one specific product. It rises fast and may change the product on a rapid time scale. Its product is a system (on the chip) rather than a commodity chip for numerous other systems. The separation from Foundry frees the packager for high-risk innovations.

The economic role of a "Packager" is actually quite similar to that of a contemporary system design house that gives orders to Si foundries for custom chips. The distinguishing features of this type of enterprise are as above: risk, innovation, and entrepreneural proprietary nature of the product.

Second basic question: *should the Foundry and the multiplicity of Packagers form one economic unit ?* We believe the answer is negative.

Proprietary aspects and rights to a new product reside with the Packager, while the Foundry perform service available to everybody. In our vision, the Packagers will order new products from the Foundry by using predetermined standards via internet. The full utilization of the Foundry capabilities by external users mandates that all technologies used at the Foundry be transparent to the users. The Foundries will be protected against competitors mainly by two entry barriers (see Porter, 1980): the economy of scale and high costs for capital requirements to start a new Foundry.

In contrast, Packager's activity may be quite opaque and protected by patents and trade secrets. This separation will be cost-effective because it encourages competition between Packagers and invites new Packagers to enter the market. These new Packagers create additional products and generate new business for the Foundry.

The separation between the Foundry and Packagers provides advantages for the Foundry because new Packagers increase the economy of scale for the Foundry. The existence of the Foundry provides the advantages of the relatively low entrance costs for Packagers because the do not have to invest in Si processing technologies and they can focus on hybrid technologies and proprietary systems that use them.

At this point let clearly recognize the counter arguments in favor of both the Si CMOS processing and the foreign semiconductor incorporation be done within the same the same economic unit. Arguments that suggest this may be the economic organization of superior efficiency may include the following considerations:

(i) if the Foundry is separate from the system house, its competitors have easier entrance to the market because the Foundry technologies contain little or no secrets within the industry;

(ii) profits per unit of production are much higher for system chips than for commodity chips.

Exact economic conditions (e.g., the demand on hybrid chips, product variety, amounts of investments) that will create incentives to the Foundry to make its technologies known to all users, are not clear and should be investigated. Of the many factors influencing the economic decision, we shall concentrate on the demand for the variety of chips generated by independent Packagers. We believe that independent Packagers driven by their entrepreneurial spirit will create a higher variety of on-chip systems. New products will increase the demand. In the next section we consider a simple mathematical model based on cost-volume analysis. This model demonstrates that if the proliferation of independent Packagers significantly increases the demand, then the structure with a Foundry and independent Packagers becomes more profitable for the VLSI manufacturer. Moreover, it creates a higher entrance barrier for competition compared to the economic regime when the same company produces on-chips devices from the beginning to the end.

3. Cost-Volume Model

Let there be I types of hybrid on-chip devices, $i = 1, 2, \ldots, I$, and let index 0 correspond to the standard VLSI processing. We denote by D_i be the demand for a particular type of a product, $i = 0, 1, \ldots, I$. For simplicity, we assume there is no waste in hybrid technologies, i.e. all non-defective silicon chips are used to create on-chip systems and their supply is equal to the demand. It means that

$$D_0 = \sum_{i=1}^{I} D_i.$$

This assumption is not far off the mark, if we include designers of proprietary chips in the same group as "Packagers".

We also assume for the sake of simplicity that each type of devices corresponds to a manufacturing facility. In reality, of course, different facilities may produce similar devices and one facility may produce several types of devices. This assumption, however, is not restrictive for our analysis because we can introduce fictitious facilities and fictitious products.

Let r_i and c_i be respectively the revenue and cost per unit for each type of production and let A_i be the fixed costs for facility i, $i = 0, 1, \ldots, I$. We assume that $A_i(D_i)$ is an non-decreasing step function such that $A_i(D_i)/D_i$ is decreasing in D_i, $i = 1, \ldots, I$. In general, the last condition may not hold, but if the demand is high, the fixed costs can be approximated by a function with this property.

If we consider the scheme when the Foundry and Packagers act as independent businesses, we have that the profit for each participant is

$$P_i = (r_i - c_i)D_i - A_i(D_i), \qquad i = 0, 1, \ldots, I.$$

The cost of entry for the Foundry is

$$E_0 = \alpha c_0 D_0 + A_0 D_0,$$

where $\alpha \in [0, 1]$ is a fraction of variable costs needed for entry.

One the other hand, in the scheme where one manufacturer of on-chip systems is responsible for both the Si chip production and the packaging, then the number of possible hybrid systems will be significantly smaller. Let us assume that only the first J types of units be manufactured in this case, $J \leq I$, and let the new demand be

$$D_0' = \sum_{i=1}^{J} D_i.$$

In this scenario we find that the profit is given by

$$P = (r_0 - c_0)D_0' + \sum_{i=1}^{J}(r_i - c_i)D_i - A_0(D_0') - \sum_{i=1}^{J} A_i(D_i)$$

and the cost of entry is

$$E = \alpha(c_0 D_0' + \sum_{i=1}^{J} c_i D_i) + A_0(D_0') + \sum_{i=1}^{J} A_i(D_i).$$

In order to simplify the formulae for P_0, P, E_0, and E, we introduce additional assumptions. Let the costs, revenues, and demands be equal for all possible hybrid facilities, i.e. $c_i = c_1$, $A_i = A_1$, $D_i = D_1$, and $r_i = r_1$ for all $i \geq 1$. Then

$$P = (r_0 + r_1 - c_0 - c_1)JD_1 - JA_1(D_1) - A_0(JD_1),$$

$$E = \alpha(c_0 + c_1)JD_1 + JA_1(D_1) + A_0(JD_1),$$

and

$$P_0 = (r_0 - c_0)ID_1 - A_1(ID_1),$$

$$E_0 = \alpha c_0 ID_1 + A_0(ID_1).$$

We observe that $\mathbf{P}(I) = (r_0 - c_0) - A_0(JD_1)/I$ is the profit per chip at the standard VLSI processing stage of production. $P(I)$ is a nondecreasing function because $A_0(JD_1)/I$ is nonincreasing. The condition that $P(I) \leq 0$ for all I means that for any possible volume the silicon chip production is not profitable. It is always possible to increase the revenue per chip r_0 and make $P(I) > 0$. If this level r_0 is too high it means that there is no economic conditions for the hybrid production.

Therefore, it is natural to assume $\mathbf{P}(I_0) > 0$ for some $I_0 > 0$. This implies that $\lim_{I\to\infty} \mathbf{P}(I) > 0$ and $\mathbf{P}(I) > 0$ for all $I \geq I_0$.

We have that $E_0 \geq E$ for $I \geq I_1$, where I_1 is any number such that

$$I_1 \geq \frac{\alpha(c_0 + c_1)JD_1 + JA_1(D_1) + A_0(ID_1)}{\alpha c_0 D_1 + A_0(I_1 D_1)/I_1}.$$

For example, we can select

$$I_1 = \frac{\alpha(c_0 + c_1)JD_1 + JA_1(D_1) + A_0(ID_1)}{\alpha c_0 D_1} < \infty.$$

Let $I \geq I_0$. Then $P_0 \geq P$ for $I \geq I_2$, where I_2 is any number such that $I_2 \geq I_0$ and

$$I_2 \geq \frac{\max\{0, (r_0 + r_1 - c_0 - c_1)JD_1 - JA_1(D_1) - A_0(JD_1)\}}{\mathbf{P}(I_2)}.$$

We observe that this finite number I_2 exists. Indeed, if the numerator in the last expression is 0 then we can set $I_2 = I_0$. Otherwise, we consider the function $F(I) = I\mathbf{P}(I)$. We have that $F(I) \to \infty$ as $I \to \infty$. Thus, the inequality holds if I_2 is large enough.

Therefore, if $I \geq \max\{I_0, I_1, I_2\}$, the structure with a Foundry and independent Packagers provides higher profits for Si chip manufacturers and higher entrance barriers for its competitors.

5. Conclusions

We have considered recent trends in semiconductor chip manufacturing. In agreement with a number of forecasters, we believe these trends suggest that the microelectronics industry is at the threshold of revolutionary changes. One of the anticipated elements of the new economic order will be the transition to a high-volume production of hybrid on-chip systems. This change will result in the creation of new entities in the semiconductor industry, dubbed here the hybrid packagers, whose role is somewhat reminiscent of the present-day system houses involved in the proprietary chip design. We have analyzed two distinct ways these new entities can be organized: one when they become parts of a larger economic unit involving the mature silicon production, the other when they form a multiplicity of independent entrepreneurial units interacting with a large Si Foundry that produces custom units on order based on common technology. We introduced a simple mathematical model that identifies economic conditions when either scheme provides higher profits to the Foundry and higher entry barriers to its competitors.

Acknowledgments. The authors thank Christopher L. Tucci for interesting comments. Research of the first author was partially supported by NSF Grant DMI-9500746.

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