# Switching in NERFET Circuits

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*Abstract*—**NERFET is a three-terminal device possessing a pronounced negative differential resistance due to the effect of real-space hot-electron transfer. The device structure, substantially modified compared to our earlier reports, gives an improved performance at room temperature. In this work, logic operation of a circuit formed by two NERFET's is demonstrated for the first time. Sharp switching of output voltage is observed. Using this circuit, we have demonstrated the operation of an inverter and a bistable switch. Under certain bias configurations the circuit also exhibits a tristable behavior which can be used for ternary logic.**

TWO-TERMINAL negative differential resistance (NDR) devices have long been considered [1], [2] for logic applications. Two NDR devices in series form a bistable element. In a certain range of external bias, this element has two stable configurations in which one of the devices takes nearly all of the applied voltage, that is, to say, contains a high-field domain. Logic operation consists of moving the domain from one device to the other by a specially designed external circuitry. Recently, we demonstrated [3] a *three-terminal* device (NERFET) in which a pronounced NDR characteristic in the source-to-drain circuit is controlled by a third electrode. Such an element offers new possibilities for logic, as described below.

The NERFET structure studied in this work is different from that used earlier. The device cross section and the energy-band diagram are shown in Fig. 1(a). The MBE grown device contains two conducting layers separated by a potential barrier. One of these layers (the "channel") consists of a two-dimensional electron gas (2-DEG) at an undoped GaAs/AlGaAs interface. The second conducting layer is made of a 0.86-$\mu$m-thick Si-doped GaAs ($N_D = 2 \times 10^{18}$ cm$^{-3}$) layer grown on a semi-insulating GaAs substrate. The barrier separating the two conducting layers is 1400 Å thick and comprises a 15-period $Al_xGa_{1-x}As$ superlattice consisting of layers with $x = 0$ (18 Å) and $x = 0.53$ (75 Å). The superlattice barrier was used to enhance the quality of the 2-DEG at the interface. Two contacts to the channel ($S$ and $D$) were nominally spaced 2 $\mu$m apart, and made of Au–Ge–Ag–Au alloy. Contact to the second conducting layer (SUB) was provided by a Au–Ge–Ni–Au alloy. In contrast to our earlier work, the SUB contact in this work was accessed from the surface individually for each device.

As indicated in Fig. 1(a), in equilibrium the channel is not conducting, being depleted by the surface field. The 2-DEG is induced at the heterojunction interface at sufficiently high $V_{SUB} > 0$. The second conducting layer therefore acts as a buried FET gate, as will be described elsewhere in detail. The rectangular shape of the barrier provides more insulation between the two conducting layers, as compared to the triangular-shaped barrier used before [3], [4]. Fig. 1(b) shows the $S$ to SUB current–voltage characteristics at 300 and 77 K. We see that even at room temperature the barrier is blocking in both directions for $V_{SUB} \lesssim 1.5$ V.

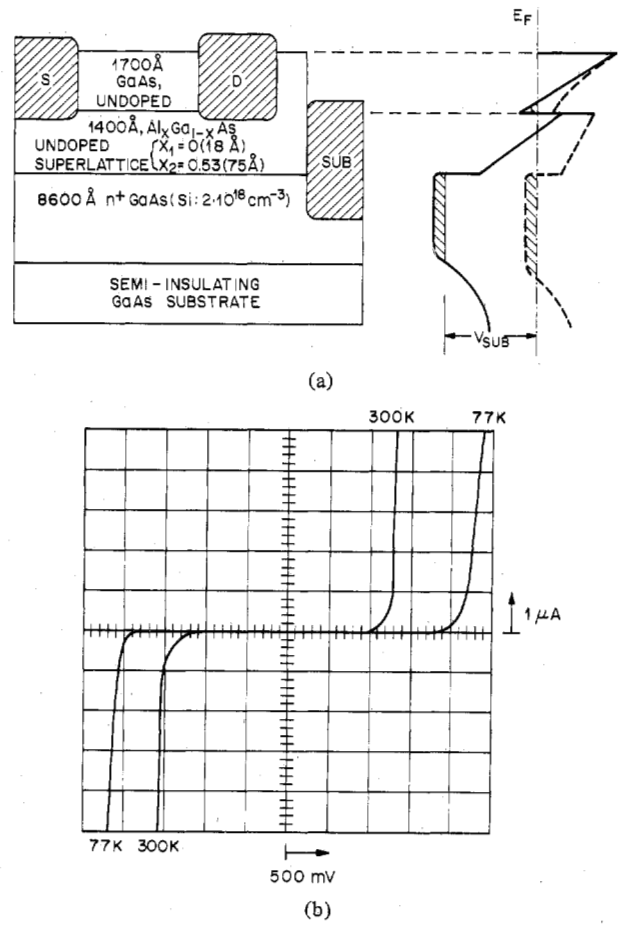


Fig. 1. Rectangular-barrier NERFET without modulation doping. (a) Cross section of the device structure. The energy-band diagram on the right-hand side illustrates two regimes: equilibrium (dashed line) and the operating mode (solid line) in which conducting channel is induced by a positive $V_{SUB}$. (b) Curve-tracer characteristics $I_{SUB}$ versus $V_{SUB}$ at 300 and 77 K; both $S$ and $D$ terminals are grounded.

Source–drain characteristics of the NERFET at room temperature and different $V_{SUB}$ are shown in Fig. 2. The device exhibits NDR for $V_{SUB} \gtrsim 2.2$ V. At $V_{SUB} = 3.2$ V,

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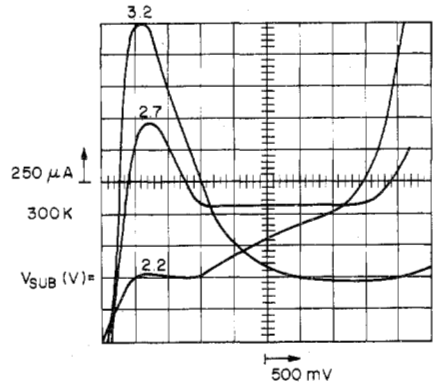


Fig. 2. Source-drain characteristics $I_D$ versus $V_D$ at room temperature for three different $V_{SUB}$. The $S$ electrode is grounded. Several selected devices had nearly identical characteristics.

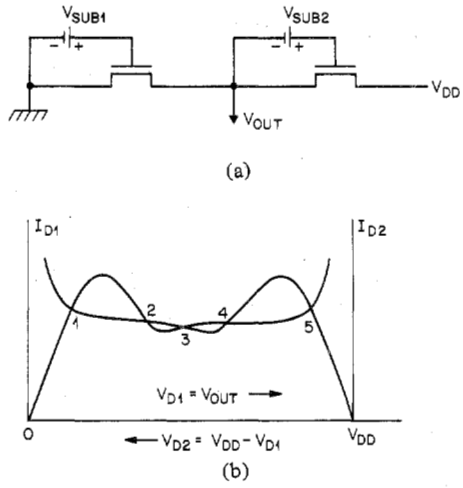


Fig. 3. A two-NERFET logic circuit. (a) Circuit diagram. (b) Graphical construct for determining the operating points. Points 1, 3, 5 are stable, points 2, 4 unstable.

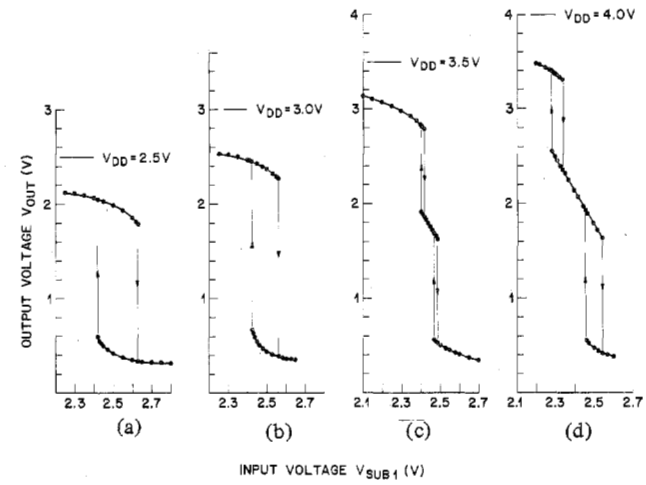


Fig. 4. Logic transitions in the circuit of Fig. 3(a) at room temperature. The output voltage $V_{OUT}$ was measured as a function of $V_{SUB1}$ slowly varied in the direction shown by arrows. Presented results correspond to a fixed $V_{SUB2} = 2.5$ V for 4 different values of $V_{DD}$.

the peak-to-valley ratio is about 5. Two devices having identical characteristics were connected in series as shown in Fig. 3(a). We designate NERFET's using conventional FET circuit symbols—with the understanding that the SUB electrode plays the role of a gate. It is clear that if the total voltage $V_{DD}$ applied to two NERFET's in series exceeds twice the critical voltage for the onset of NDR, then an instability occurs in which one of the devices is expected to take most of the applied voltage. By changing the controlling voltages $V_{SUB1}$ and/or $V_{SUB2}$ we can shift the high-field domain from one device to the other, thus providing the basis for logic operations.

Examples of such an operation are shown in Fig. 4. One of the controlling voltages is kept constant $V_{SUB2} = 2.5$ V while the other $V_{SUB1}$ is varied. We see that at certain values of the controlling voltage $V_{SUB1}$, the system exhibits instabilities with the output voltage $V_{OUT}$ switching from a low ($V_{OUT} \sim 0.4$ V) to a high ($V_{OUT} \sim V_{DD} - 0.4$ V) state and back. As $V_{SUB1}$ is varied, the system smoothly approaches the switch points—which are sharply defined and highly repetitive (within 1 mV). Such a behavior with a strong hysteresis is reminiscent of a phase transition. At fixed $V_{SUB2} = 2.5$ V and $V_{DD} \lesssim 3.5$ V the transition from low to high states is independent of $V_{DD}$ and occurs at $V_{SUB1} = 2.424$ V (see Figs. 4(a),(b)). The width of the hysteresis decreases with increasing $V_{DD}$. At $V_{DD} \gtrsim 3.0$ V, the output swing of the inverter is capable of switching a second inverter without any level shifting, so that direct coupling of inverters, such as in a ring oscillator, is possible. At $V_{DD} > 3.5$ V one sees a new feature: the appearance of a third stable state characterized by $V_{OUT}$ being in a range near $V_{DD}/2$. Within this range the dependence $V_{OUT}$ versus $V_{SUB1}$ is strictly linear (with a voltage gain of nearly 4) and nonhysteretic (Figs. 4(c), (d)). To our knowledge [5], a tristable operation with a stable midpoint has never been observed with two series-connected voltage-controlled NDR elements. The operating points of the two-NERFET system can be determined from the characteristics of Fig. 2 by the usual load-line graphical construct in Fig. 3(b). In our view, the stable midpoint (point 3 in Fig. 3(b)), which appears only at a sufficiently high $V_{DD}$, results from an intersection of positive slopes in the $I$–$V$ characteristics of both devices.

Behavior similar to that illustrated in Fig. 4 was seen for other fixed values of $V_{SUB2} \leqslant 2.65$ V. On the other hand, for $V_{SUB2} > 2.65$ V it was not possible to return the system to its low state by varying $V_{SUB1}$. In this case we had to temporarily lower $V_{SUB2}$ in order to move the high-field domain to device 2 (which corresponds to the low state of the system). After that we could bring the system back to the high state by temporarily lowering $V_{SUB1}$.

We now return to the experimental situation corresponding to Figs. 4(a) and (b). Two types of logic operation can be thought of in this configuration. Firstly, we can dc prebias our input voltage to a value in the middle of the hysteretic loop, say, $V_{SUB1} = 2.5$ V in the instance of Fig. 4(b). Applying controlling signals $\Delta V_{SUB1}(t)$ in the form of a series of short low-amplitude ($|\Delta V| \gtrsim 0.15$ V) pulses of varying polarity, we then have a *bistable element:* the system will "remember" the sign of the last pulse, viz. $V_{OUT}$ = high for $\Delta V < 0$ and $V_{OUT}$ = low for $\Delta V > 0$. A second type of logic

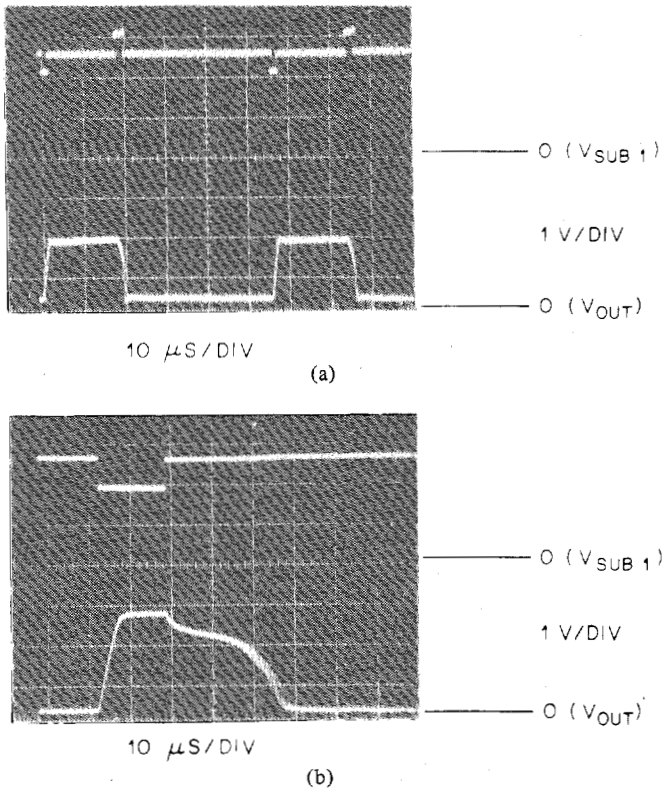


Fig. 5. Oscilloscope traces of logic operation in the circuit of Fig. 3(a) at $T = 300$ K: (a) bistable switch: $V_{DD} = 2.6$ V, $V_{SUB2} = 2.49$ V, $V_{SUB1} = 2.55$ V + $\Delta V_{SUB1}(t)$; (b) inverter: $V_{DD} = 3$ V, $V_{SUB2} = 2.52$ V, $V_{SUB1} = 2.65$ V + $\Delta V_{SUB1}(t)$. In both photographs the top trace corresponds to the input pulses and the bottom trace to $V_{OUT}$.

operation—*inverter* action with amplification—can be obtained by dc prebiasing $V_{SUB1}$ to high enough voltages ($V_{SUB} \gtrsim 2.6$ V for Fig. 4(b)) to ensure a stable low state. The system will then switch to its high state only during a pulse of negative polarity $|\Delta V_{SUB1}| \gtrsim 0.2$ V.

These logic operations are demonstrated in Fig. 5. Fig. 5(a) shows the operation of a switch with two stable states $V_{OUT} \approx 0.4$ V and $V_{OUT} \approx 2$ V. Switching occurs under sequential applications of pulses $\Delta V_{SUB1} = \pm 0.5$ V of width $\sim 2$ μs. Inverter action is shown in Fig. 5(b) where the system, normally in its low state, switches to the high state during a pulse $\Delta V_{SUB1} \approx 0.7$ V.

We believe that the relatively long switching times (2–4 μs) are due to high parasitic capacitances of our dc-bias circuitry. On the other hand, when the applied $V_{SUB1}$ approaches one of the transition points then the duration of the corresponding transition increases rapidly. The trailing edge for $V_{OUT}$ in Fig. 5(b) illustrates this effect. A fluctuation-induced nature of the transition is evident from the oscilloscope traces. As we approach the transition point closer and closer, the trailing edge widens and eventually the system snaps permanently into its high state. On the other hand, moving the system away from the transition point, e.g., by making $V_{SUB1}(\text{dc}) \gtrsim 2.7$ V, we shorten the trailing edge bringing it to approximately the same value as the rising time. This fluctuative behavior of the switch is reminiscent of noise-induced transitions [5], [6].

In conclusion, we have demonstrated a logic operation of a novel two-NERFET system at room temperature. We have shown a bistable-switch as well as an inverter-amplifier actions. The system also exhibits a tristable operation which can be used for ternary logic.

## ACKNOWLEDGMENT

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