Resonant tunneling of two-dimensional electrons through a quantum wire: A negative transconductance device

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A novel three-terminal resonant-tunneling structure is proposed in which the double potential barrier is defined within the plane of a two-dimensional (2-D) electron gas. The resonant tunneling of 2-D electrons into a 1-D "quantum wire" is controlled not only by a source-to-drain voltage but also by a gate potential. In addition to the negative differential resistance found in conventional resonant-tunneling diodes, our device offers a negative transconductance. This feature is potentially useful for low-power logic circuits.

The study of negative differential resistance devices based on resonant tunneling in double-barrier heterostructures was pioneered by Tsu, Esaki, and Chang.[1] Recently, there has been renewed interest in such devices, both experimental[2–5] and theoretical.[6–7] A three-terminal bipolar structure, utilizing resonant tunneling of minority carriers through a quantum well (QW) in the base, has also been proposed.[8] All these works dealt with the bulk-carrier tunneling into a two-dimensional (2-D) density of electron states in a QW.

In the present letter we propose a novel structure in which the QW is linear rather than planar and the tunneling is of 2-D electrons into a 1-D density of states (a "quantum wire"). We shall illustrate the idea assuming an AlGaAs/GaAs heterostructure implementation. Figure 1 shows the schematic cross section of the proposed device. It consists of an epitaxially grown undoped planar QW and a double AlGaAs barrier sandwiched between two undoped GaAs layers and heavily doped GaAs contact layers. The working surface defined by a V-groove etching is subsequently overgrown epitaxially with a thin AlGaAs layer and gated. The thickness of the gate barrier layer ($d \gtrsim 100$ Å) and the Al content in this layer ($x \gtrsim 0.5$) should be chosen so as to minimize gate leakage. The thicknesses of the QW barrier layers are chosen so that their projections on the slanted surface should be $\lesssim 50$ Å each. The Al content in these layers should be typically $x \lesssim 0.45$. Application of a positive gate voltage V_G induces 2-D electron gases at the two interfaces with the edges of undoped GaAs layers outside the QW. These gases will act as the source (S) and drain (D) electrodes. At the same time, there is a range of V_G in which electrons are not yet induced in the quantum wire region (which is the edge of the QW layer) because of the additional dimensional quantization.

Indeed, consider the band diagram in the absence of an S to D voltage, $V_D = 0$, Fig. 2(a). The diagram is drawn along the x direction (from S to D parallel to the surface channel). We shall denote by y the direction normal to the gate and by z that along the quantum wire. Dimensional quantization induced by the gate results in a zero-point energy of electronic motion in the y direction, represented by the bottom E_0 of a 2-D subband corresponding to the free motion in x and z directions. The thicknesses of the undoped S and D layers are assumed large enough ($\gtrsim 1000$ Å) that the electronic motion in x direction in these layers can be considered free. On the other hand, in the QW region of the surface channel there is an additional dimensional quantization—along the x direction—which defines what we call the quantum wire.[9] If we denote by t the x projection of the QW layer thickness, then the additional zero-point energy is approximately given by $E_0' - E_0 = \pi^2\hbar^2/2m^* t^2$ (this is a good approximation, provided the barrier heights substantially exceed E_0'). Application of a gate voltage moves the 2-D subband E_0 with respect to the (classical) bottom of the conduction band E_C and the Fermi level E_F. The operating regime of our device with respect to V_G at $V_D = 0$ corresponds to the situation when E_F lies in the gap $E_0' - E_0$.

Application of a positive drain voltage V_D brings about the resonant-tunneling condition, illustrated in Fig. 2(b). In this situation the energy of certain electrons in S matches unoccupied levels in the quantum wire. Assuming conservation of the lateral momentum k_z during tunneling, only those electrons whose momenta lie in a segment $k_x = k_x^0$, where $\hbar^2(k_x^0)^2/2m^* = \Delta$, can participate in resonant tunneling. The resonant segment is shown in Fig. 2(c). The energies of all electrons in this segment lie in the band $E_0 + \Delta \leqslant E$

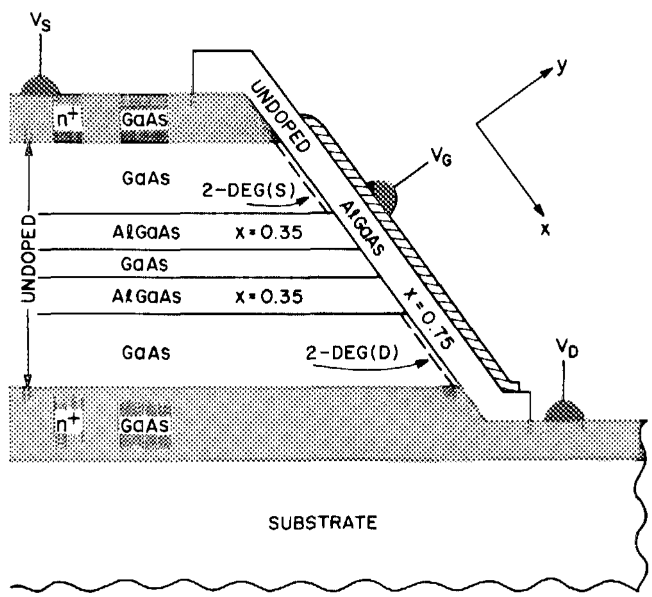

FIG. 1. Schematic cross section of the proposed surface resonant tunneling device structure. Thicknesses of the two undoped GaAs layers outside the double-barrier region should be sufficiently large ($\gtrsim 1000$ Å) to prevent the creation of a parallel conduction path by the conventional (bulk) resonant tunneling.

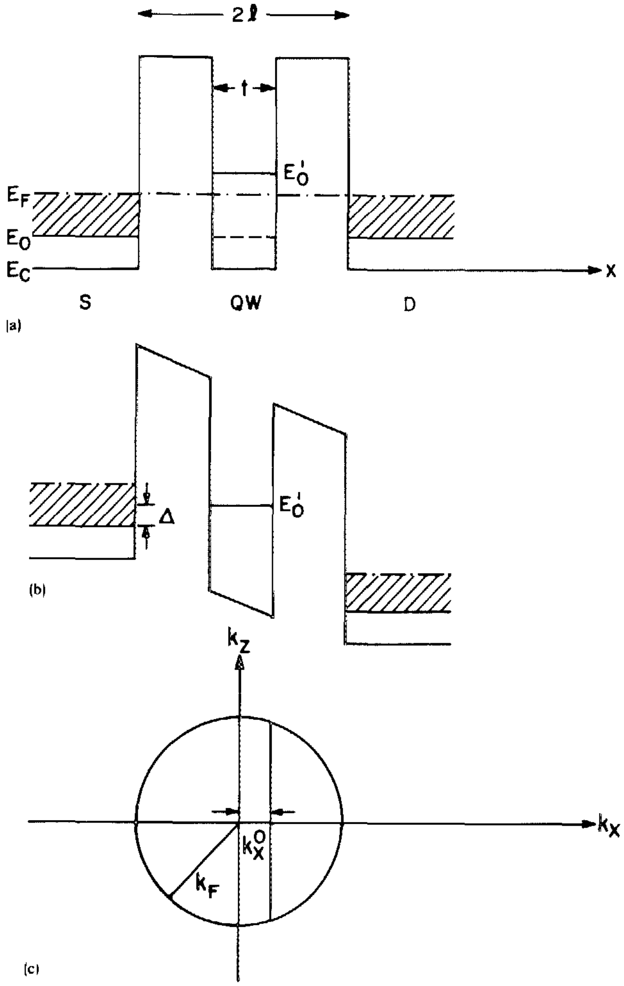

FIG. 2. Illustration of the device operation. (a) Band diagram along the channel in "equilibrium," i.e., in the absence of a drain bias. (b) Band diagram for an applied bias V_D, when the energy of certain electrons in the source (S) matches unoccupied levels of the lowest 1-D subband E_0' in the quantum wire. (c) Fermi disk corresponding to the 2-D degenerate electron gas in the S electrode. Vertical chord at $k_x = k_x^0$ indicates the momenta of electrons which can tunnel into the quantum wire while conserving their momentum k_z along the wire.

$\leqslant E_F$, but it should be clearly understood that not all the electrons in that energy band are resonant because of the momentum conservation. As V_D increases, the resonant segment moves to the left, Fig. 2(c), toward the vertical diameter $k_x = 0$ of the Fermi disk, and the number of tunneling electrons grows, reaching a maximum $[2m^*(E_F - E_0)]^{1/2}/\pi\hbar$ per unit length in the z direction when $\Delta = 0$. At higher V_D when $\Delta < 0$, there are no electrons in the source which can tunnel into the quantum wire while conserving their lateral momentum. This gives rise to a negative differential resistance in the drain circuit. The described mechanism of the negative resistance is analogous to that discussed earlier[7] for the case of tunneling into a 2-D density of states, as in the conventional "planar" QW structures.[1–5] The present structure, however, offers a fascinating possibility of controlling resonant tunneling by the gate voltage, as we shall now discuss.

This control is effected by the fringing electric fields, illustrated in Fig. 3. Electrostatically, our structure is equivalent to a double parallel-plate capacitor with one common (gate) electrode. The separation between the parallel plates, d, equals the thickness of the AlGaAs gate-barrier layer, and the slit width, $2l$, corresponds to the combined thicknesses of the two tunneling-barrier layers and the QW layer, projected on the x direction. First consider the effect of the drain voltage, which we have already described qualitatively above. Assume $V_G = V_S = 0$ and $V_D > 0$. For simplicity of the calculation we assume a "normally-on" device, i.e., the existence of a 2-D electron gas in S and D regions in the absence of a positive gate bias. This electrostatic problem is solved by a conformal mapping of the domain shown in Fig. 3 (bottom left), corresponding to the complex plane $\zeta \equiv x + iy$, onto a simple strip (bottom right) $0 < \mathrm{Im}(\phi) < V_D$ in the "potential" complex plane $\phi \equiv \xi + i\psi$. This mapping is performed by the function[10]

$$z = b - \exp(-V_D\phi/\pi) + d\ln[1 - 2b\exp(-V_D\phi/\pi)], \quad (1)$$

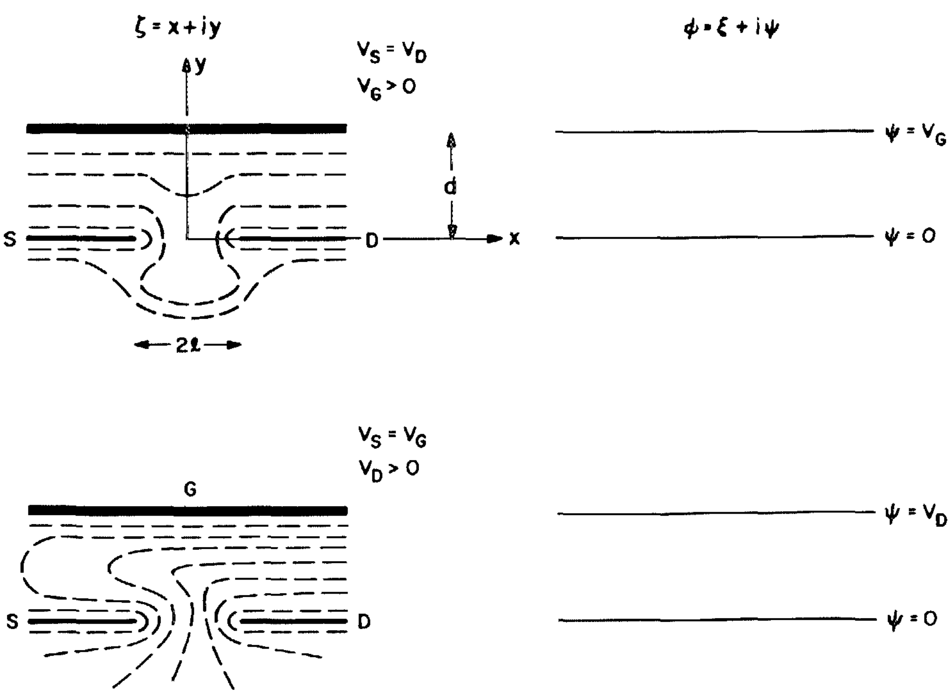

FIG. 3. Electrostatic potential distribution in the surface resonant tunneling structure. Figures on the left show the cross section of the device in the plane perpendicular to the quantum wire, modeled as a domain in a complex ζ plane, and the projections of equipotential surfaces (dashed lines) for two different bias configurations. The slit width $2l$ is the combined thickness of the double barrier and the well projected on the channel direction (x axis), and d is the gate-barrier thickness. Figures on the right describe the domains in the complex ϕ plane obtained by the conformal mappings, Eqs. (1) (bottom figure) and (3) (top figure).

where

$$b = d(\rho^2 + 1)^{1/2} - d, \tag{2a}$$

and ρ is the real root of the equation

$$\rho + \ln[\rho + (\rho^2 + 1)^{1/2}] = l/d. \tag{2b}$$

The potential $\psi(x, y)$ at any point is given by the imaginary part of $\phi(z)$. The resultant projections of the equipotential surfaces on the xy plane are shown in Fig. 3 by the dashed lines. Next we consider the effect of the gate. We now assume $V_S = V_D$ and $V_G > 0$. In this problem the physical domain (Fig. 3, top left) is conformally mapped on the strip $0 < \mathrm{Im}(\phi) < V_G$ (Fig. 3. top right) by the following transformation:

$$z = b \tanh(V_G \phi / 2\pi) + V_G \phi d / \pi - ilV_G, \tag{3}$$

where b is still given by (2a).

Analysis of Eq. (1)–(3) shows that for $d \approx l$ the gate potential is nearly as effective in lowering the E_0' level in the quantum wire with respect to E_0 in the source as is the drain potential. Of course, the real operating regime involves the situation in which both $V_G > 0$ and $V_D > V_S$, when no suitable conformal mapping onto a simply connected domain is available. However, it is clear that the effects described in Fig. 3 can be treated as additive, at least qualitatively. This means that we can control by the gate potential the resonant-tunneling condition set up by the source-to-drain voltage. If we start from the situation with $\Delta \gtrsim 0$ at a fixed V_D, we can then make $\Delta < 0$ by increasing V_G, thus quenching the tunneling current. This implies the possibility of achieving the *negative transconductance*—an interesting feature in a unipolar transistor. Such a transistor can perform the functions of a complementary device analogous to a p-channel transistor in the silicon CMOS logic. A circuit formed by a conventional n-channel field-effect transistor and our negative transconductance device can act like a low-power inverter in which a significant current flows only during switching. This feature can find important applications in GaAs logic circuits.

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