distribution, the SLS requirement of decreasing r leads to less efficient absorption at the peak intensity, thus more than offsetting the gain.

Setting $\Gamma = 1/2$ in Equation 41 with $h \rightarrow h_{SLS}^{MAX}$, taking $\lambda = 1.3\ \mu m$ and $x = 0.6$, and using Equation 43, we find

$$h_{SLS}^{MAX} = 1340\ \text{Å}/\sqrt{r} \tag{45}$$

Substituting this into Equations 39 and 40 yields a transcedental equation for r, namely, $36.3r^{3/2} = \ln(335/\sqrt{r})$ with the solution $r \approx 0.3$, corresponding to $h_{SLS}^{MAX} \approx 2400$ Å. Thus, we can expect an optimum value* $\alpha_{eff} \leq 0.2\alpha \approx 20\ cm^{-1}$ in an SLS consisting of 12 periods of 60 Å Ge_xSi_{1-x}/140-Å Si.

This means that the waveguide length must be of the order of 0.5 mm for high speed detector efficiency. If a *pin* detector represents a ridge waveguide of that length and the width $\lesssim 10\ \mu m$, then its capacitance is less than about 0.5 pF, assuming a typical depletion width of 1 μm. This value of the internal capacitance is acceptable and comparable to that of the conventional *pin* IR detectors. Note that the detector quantum efficiency grows with the optical path length, without degrading the speed of response.

The detector sensitivity will be further improved by an avalanche gain in Si cladding layers. To reduce an excess noise, the APD design should be guided by the following principles:

1. Since $K \equiv \alpha_n/\alpha_p >> 1$ in Si, the multiplication should be initiated by electrons rather than holes.
2. Since K decreases sharply when the electric field much exceeds the ionization threshold, E_i, the field in the avalanche layer should be near the threshold, $E \gtrsim E_i \approx 3 \times 10^5$ V/cm, and the thickness of that layer should be well above $\alpha_n^{-1}(E_i) \approx 0.5\ \mu m$.
3. The field in the SLS layers should not exceed approximately 10^5V/cm, the ionization threshold in Ge.

A possible waveguide APD structure is illustrated in Figure 26. In addition to an undoped Ge_xSi_{1-x}/Si SLS of $x \gtrsim 0.6$, $r \lesssim 0.3$ and thickness $h_{SLS} \gtrsim 3000$ Å, it contains an undoped Si avalanche layer of thickness $d \gtrsim 2\ \mu m$ separated from the SLS by a thin ($\Delta \lesssim 10^{-6}$ cm) *p*-type Si layer. In the operating regime, the Δ-layer must be depleted by an applied reverse bias. The total sheet density of charge in this layer should, therefore, be of order $\kappa E_i \approx 2 \times 10^{12}\ e/cm^2$. This will achieve the desirable high-low field separation of the absorption and multiplication layers and result in a low-noise SAM APD structure. Development of Si-based detectors for fiber-optical communications represents one of the most practical applications of Si-MBE research.

B. Epitaxial Insulators

Research in the growth and characterization of epitaxial insulators on semiconductors has undergone a rapid expansion in recent years. Besides the obvious scientific interest in understanding the properties of a single-crystal semiconductor/insulator interface, this research has many motivations from the point of view of device applications. In III-V compounds, one is strongly interested in implementing a basic MIS structure for use in insulated-gate field-effect transistors (IGFET). In silicon one has hopes for improving the transport

* It should be noted that strain-symmetric superlattices, grown on a relaxed layer of intermediate composition,[85] are not subject to any restriction on the possible SLS thickness. These structures may be of interest for the implementation of waveguide detectors — provided dislocations propagating from the buffer layer do not continue to thread the SLS (otherwise they would again degrade the detector operation by contributing to the dark current at room temperature).

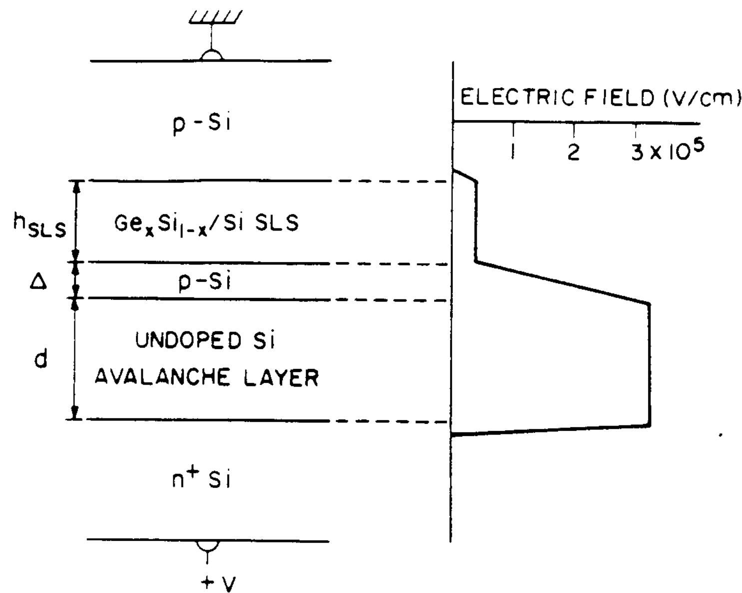

FIGURE 26. A waveguide APD structure and the electric field profile.

properties in the inversion layer at an ordered interface, compared to that at an MOS interface. There is also a great interest in fabricating a silicon-on-insulator (SOI) structure, which would allow the implementation of MOSFETs with improved speed characteristics and single-event upset immunity, as well as complementary (CMOS) circuits without latchup.

Since the pioneering work of Farrow et al.[94] and Ishiwara and Asano,[95] a great deal of epitaxial-insulator research has been centered on the growth of epitaxial fluorides, such as CaF_2 on silicon and epitaxial silicon on the fluoride layers. A review of the recent accomplishments in this field can be found in Chapter 6 by Phillips and Chapter 5 by Ishiwara in this book. In the next section we shall discuss some of the device aspects of the SOI program. Ultimately, this development may lead to three-dimensional integration of Si circuits with improved packing density of transistors and shortened intrachip communication lines. Moreover, the development of a single-crystal SIS material structure may provide researchers with a unique system of two-dimensional electron and hole gases, spatially separated but coupled electrostatically through a thin insulator. As will be discussed in Section III.B.2, such a system may possess remarkable novel properties. Another interesting possibility, which we shall not discuss, entails the use of epitaxial insulators on silicon as an electron-beam resist with higher fine-line resolution than that available with conventional polymer or polycrystalline layers.[96,97]

1. SOI and Three-Dimensional Integration

SOI technologies for MOSFET applications have been long sought by various means, including beam-anneal recrystallization of polycrystalline silicon layers deposited on amorphous SiO_2 films,[98,99] heteroepitaxial growth of silicon on sapphire[100] and spinel films,[101] seeded solidification of Si films over SiO_2 by lateral epitaxy,[102] lateral oxidation of porous single-crystal Si layers underneath epitaxial Si films,[103,104] and heteroepitaxial growth of Si/CaF_2 systems.[105] Potentially, these technologies offer several advantages over conventional bulk-silicon processes. The lower parasitic junction capacitance in SOI devices allows their faster operation with lower power dissipation. The greatest advantages are expected in CMOS VLSI applications.[106] The use of insulating substrates leads to a simpler fabrication sequence and enables a higher device packing density with complete immunity to latchup. The SOI

devices are, moreover, expected to possess increased radiation hardness and immunity to single-event upsets. Many investigators are also attracted by the vision of three-dimensional integration of VLSI circuits; with improvements in film quality the basic SOI layers can be stacked to form multilayer device structures. Let us briefly discuss some of these and other possible advantages from the point of view of a device physicist.

First, consider the possibility of improving the basic MIS Si structure by using epitaxial insulators instead of the amorphous silicon dioxide. Due to the ordered nature of the interface, one can possibly expect an enhanced electron mobility in the inversion layer. It should be noted that the mobility itself is not an important figure of merit in fine-line FET devices with feature sizes of 1 μm and less. A much more significant parameter is the saturated electron drift velocity, v_S. However, there seems to exist a correlation between the improved mobility and an enhancement of v_S in two-dimensional electronic systems. For example, in GaAs HEMT devices the saturated electron velocity ($v_S = 2 \times 10^7$ cm/sec at 300 K and 3×10^7 cm/sec at 77 K)[6] appears to be higher than that in bulk GaAs. It remains to be seen whether a similar enhancement can be established in epitaxial silicon/insulator systems.

Another improvement could be associated with a remote possiblity of achieving a higher density of charge in the Si inversion layer. In MOS structures this density is limited by the dielectric permittivity $\kappa_{OX} = 3.9$ and the breakdown field $E_{br} \approx 10^7$ V/cm of silicon dioxide to a value of $\kappa_{ox} \times E_{br} \approx 2 \times 10^{13}$ e/cm^2. Although CaF_2 has a higher permittivity (κ_d = 6.8) than SiO_2, the measured dielectric strength in CaF_2 layers is only 3×10^6 V/cm.[105] Higher density of charge in the inversion layer is desirable for FET circuits because it enhances the current drive at a given gate width of a transistor and thus diminishes the delay due to parasitic capacitances.

Next, let us comment on the SOI program. We shall make a rather long-shot assumption that the material quality in epitaxial Si layers will eventually match that available in bulk silicon. It is still not at all clear that the traditional speed advantage of SOI transistors, predicted on the basis of long-channel device analysis, will stand up to downward dimensional scaling of the conventional bulk-silicon MOSFETs. As the device dimensions shrink, the significance of parasitic drain-to-bulk junction capacitances can be expected to diminish, while that of interdevice capacitive "cross-talk" can be expected to increase. The SOI configurations appear to be unfavorable in this regard. Furthermore, the absence of a bulk contact is known to produce unwelcome characteristics, such as the "kink effect" (Reference 14, page 493). An encouraging, though certainly not definitive, answer to such concerns was recently given by a direct comparison of the characteristics of fine-line MOS circuits, fabricated under identical design rules on both insulating (sapphire) and bulk-silicon substrates.[106] Clearly, the immunity to latchup in CMOS applications is the single most important potential advantage of SOI technologies.

Considering three-dimensional integration, one should be very cautious in projecting the possibilities of achieving an increased device packing density in this way. At present, this density is limited not so much by the available real estate on the chip as by the power dissipation. To appreciate how awesome this problem is, let us assume that the entire CMOS chip area is covered with FET gates, the gate oxide thickness is 100 Å, the voltage swing is 2 V, and each transistor is switched on an average of once every nanosecond. This rather mild example (no parasitic capacitances, relatively slow speed for VLSI of the future) implies the generation of heat at the rate of more than 1 kW/cm^2. The critical problem in achieving super-high packing densities is to reduce the operating voltage swing (heat production scales as V^2). This in turn depends on the margin for threshold variations, which at this time is not among the strong points of SOI technologies.

2. Electron-Hole Superconductivity

Lozovik and Yudson had proposed[107] a new mechanism of superconductivity based on the pairing of spatially separated electrons and holes that arises from their Coulomb attraction.

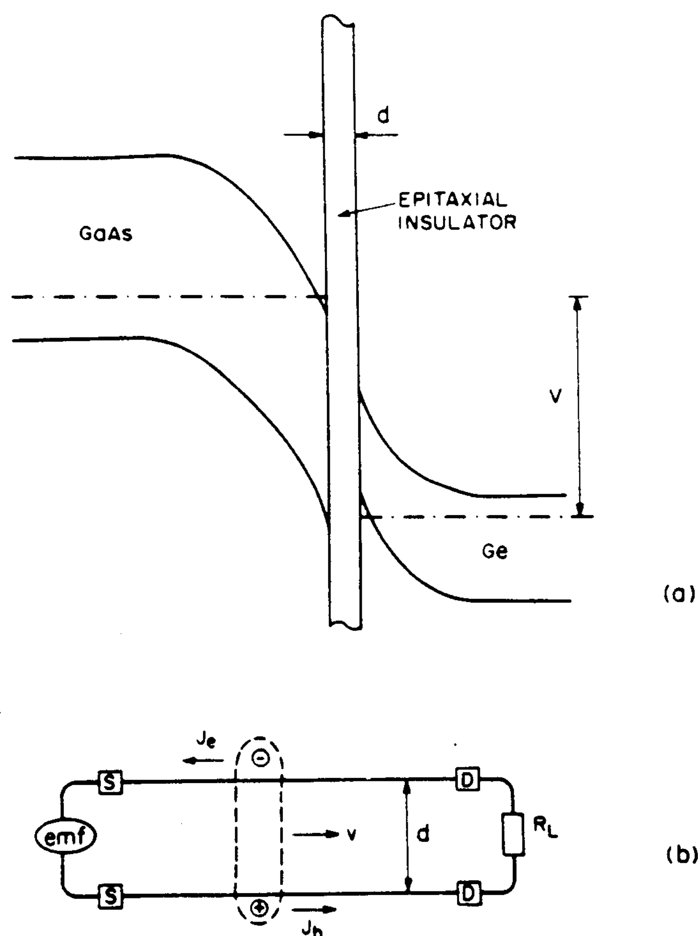

FIGURE 27. Illustration of an electron-hole superconducting system.[107] (a) Schematic band diagram involving two (possibly different) semiconductors separated by a thin epitaxial insulator with opposite-polarity carriers accumulated at the semiconductor-insulator interfaces; (b) nondissipative two-wire transmission line. (From Lozovik, Yu. E. and Yudson, V. I., *Sov. Phys. JETP*, 44, 389, 1976. With permission.)

They considered two semiconductors separated by a dielectric film of thickness d and permittivity κ_d. In such a system, one can have an accumulation of electrons on one side of the dielectric and holes on the other (Figure 27a). Tunneling through the dielectric is assumed negligible. Lozovik and Yudson (LY) suggested that the pairing interaction may lead to the formation of a new coherent state of the system in which the motion of spatially separated electrons and holes is superfluid.

According to LY, such a system will behave like a nondissipative "two-wire electric transmission line" (Figure 27b), with nonattenuating electric currents flowing in opposite directions in different parts of the system. Estimates of the transition temperature T_c to this superconducting state give much higher values than that for the usual phonon-mediated superconducting transition. This is because in the LY mechanism the pairing is caused by Coulomb interaction, which is much stronger than the phonon exchange. By the order of magnitude, $kT_c \sim m^*e^4/\kappa_d^2\hbar^2$ (assuming equal effective masses m^* for both electrons and holes). However, this estimate requires that $d \lesssim a^* \equiv \kappa_d\hbar^2/m^*e^2$ and that the surface carrier density be $\lesssim d^{-2}$. For example, if $m^* \approx 0.07\ m_0$ and $\kappa_d \approx 7$, then $a^* \approx 50$ Å and for d

$\leq a^*$ one has $T_c \sim 300$ K. It seems that the MBE of epitaxial insulators may eventually be able to provide a system which could test these theoretical predictions.*

IV. INCOMMENSURATE SILICON HETEROEPITAXY

In Section III.A.1 we discussed germanium *pin* photodetectors epitaxially grown on a <100> Si substrate. These devices represent an example of what we would like to call the incommensurate silicon heteroepitaxy approach. Generally, in this approach one does not seek to utilize any properties of the heterointerface between silicon and a foreign semiconductor, and hence the quality of that interface is not a consideration. Instead one looks for the possibility of growing high-quality layers of a desired semiconductor on silicon — with intermediate layers if necessary. The first GaAs devices (solar cells) fabricated on a Si substrate were reported by Gale et al.[108] A number of recent experimental results[109-125] on heteroepitaxial growth give us grounds to believe in the fundamental soundness of this approach.

These results clearly indicate that the fabrication of device-quality single-crystal III-V compound semiconductor layers on Si <100> substrates is possible and within reach. A closely related development is the heteroepitaxial growth of other Column IV elements (Ge, Sn) on silicon. Layers of germanium, tin, and their alloys can serve as intermediate layers facilitating the subsequent growth of III-V compounds, but also have various direct (e.g., photovoltaic) applications themselves. Of great interest, for example, is the metastable Sn_xGe_{1-x} alloy (discussed in Section IV.B), which not only can provide a perfect lattice match to various III-V compounds, but also can be expected to possess a direct gap at $x \gtrsim 26\%$. This material can be expected to have a low electron mass and high mobility, and it may also offer the possibility of fabricating LEDs and even lasers using only Column IV elements. In our view, various incommensurate-heterostructure combinations will become standard in the semiconductor industry of 1990s. A major purpose of the present section is to argue convincingly this point of view. We stress that it calls for a radical revision of directions in microelectronics. The new approach should emphasize the unity of Column IV and III-V semiconductors in the future device structures, rather than a coexistence of widely divergent technologies aimed at different applications.

In its most ambitious form, this direction requires full compatibility of the heteroepitaxial process with the conventional VLSI technology. This means that ultimately the heterolayers will form special-purpose islands in a VLSI chip. We strongly believe that such an architecture represents the future of microelectronics. A less ambitious program (which in our view is also less likely to ultimately prevail in the commercial field) is to concede the compatibility issue and be concerned instead with using silicon merely as a cheap substrate for GaAs circuits. In this case, one can use Si surfaces of orientations other than <100> and be less constrained in the growth conditions.

A. Silicon as an Inexpensive Substrate for Epitaxial GaAs Devices

The case of GaAs vs. Si has been argued for many years.[126-128] There is no doubt that today Si technology holds a dominant position in the general area of logic and memory circuits. On the other hand, the III-V compounds have many advantages: lower electron effective mass, higher mobility, the possibility of bandgap engineering, optoelectronic properties associated with the direct-gap band structure, ready availability of semi-insulating substrates, radiation hardness, etc. In the past few years, the modulation-doped GaAs/

* Another possible approach to implementing such a system is to use semiconductor heterostructures, such as $GaAs/Al_xGa_{1-x}As/GaAs$, with the accumulation of electrons and holes on opposite sides of the wide-gap layer. This approach has been pursued for some time by Kastalsky,[illegible] to whom we are indebted for an informati[illegible] discussion of the electron-hole superconductivity.

AlGaAs heterojunction transistor MODFET (also known under many names such as TEGFET or HEMT) has emerged as a serious contender for very high-speed logic circuits.[6] Recently, a group from Fujitsu[5] described the status and trends of their HEMT technology aimed at integrated circuits. Particularly impressive was the achieved control of the threshold voltage: 19-mV standard deviation over a 2-in. wafer with 0.5 μm-gate devices. It has been argued for several years that GaAs devices, such as the HEMT, may have an edge in small-signal and logic front-end applications. With the above-mentioned recently achieved threshold control, it is now argued that HEMT will become a leader in large-scale integrated circuits. Here one talks not only about large digital systems ("supercomputers") at liquid nitrogen temperatures, but also about the VLSI which so far has been a sovereign domain of silicon technology. The main obstacle (hoped to be overcome) quoted by the proponents of HEMT is the lower quality of GaAs epitaxial layers (typically 200 to 300 fatal defects per square centimeter, as contrasted with silicon 0.1 to 0.05).

In our view, a more fundamental handicap of HEMT (or any other device grown on bulk III-V compound substrates) is the cost of the material. As will be discussed in the next section, cost consideration will probably exclude bulk GaAs or InP substrates from VLSI applications. We believe that this conclusion is shared by a majority in the semiconductor industry. Most of the experts foresee a separation of markets between Si and III-V compounds — with different mature technologies catering to distinct requirements. In that view, the entire VLSI market will remain held by silicon, while the III-V compounds will be used at lower integrated levels whenever the Si technology cannot do the job — i.e., in very high speed and, especially, in optoelectronic applications. Even for those applications alone, the expected demand for GaAs is so great that some projectionists begin to worry about security of the future supply of pure gallium!

We see a different perspective. In our opinion, the winning technology will be the one that can combine the low cost of silicon with the often superior and more versatile properties of III-V materials. Such a combination can be provided by a heteroepitaxial growth of single-crystal III-V compound layers on Si substrates. These hybrid material systems will allow for the combination of high-speed GaAs devices (such as HEMT) with Si-VLSI in the form of a monolithic chip on a low-cost silicon substrate. Monolithic chips have a tremendous advantage in the cost of packaging over hybrid circuits composed of devices on separate chips. In most applications, savings will be realized from the reduction in the system's size, weight, power consumption, board costs, etc. Moreover, the advantage of hybrid material systems lies not only in the economics, but also in their potentially higher performance. For example, most of the parasitic impedances associated with interchip communication will be eliminated. In the longer run, diode lasers, LEDs, or light-intensity modulators on one end, coupled with IR detectors on the other, will form optical links for high-rate data transmission between different areas of the same chip as well as between different chips in a larger system.

1. Economic Considerations

At present, high-speed integrated circuits using MESFETs or HEMTs are fabricated on bulk compound-semiconductor wafers. This approach is not cost effective. For example, a 100-mm polished GaAs wafer costs about $400 which is over 25 times that of a corresponding Si wafer (Table 1).

As the GaAs crystal-grown and wafer-shaping operations move down the learning curve, the cost of GaAs wafers will decrease. However, the cost of a bulk GaAs wafer will never become comparable to that of Si. This is because of

1. Higher raw material cost: High-purity raw material of GaAs costs about $700/kg which is about 13 times more expensive than Si. This is due to the high costs of mining and purifying gallium and arsenic — both are scarce in the earth's crust, while Si comprises 25% of the earth's crust and is second only to oxygen in abundance.

Table 1
COST COMPARISON OF BULK Si AND GaAs WAFERS[a]

Semiconductor	Si	GaAs	Ratio of GaAs/Si
High purity raw material cost (M_1)	\$55/kg	\$700/kg	13
Volume per 100-mm wafers[b] (V)	4.32 cm³	5.89 cm³	1.36
Density (ρ)	2.33 g/cm³	5.32 g/cm³	2.28
Weight per 100-mm wafer (W = Vρ)	10.07 g	31.33 g	3.11
Raw material cost per 100-mm wafer ($M_1 \cdot W$)	\$0.55	\$21.93	40
Cost of polished 100-mm wafer (M_2)	\$15	\$400	27
Area of 100-mm wafer (A)	78.54 cm²	78.54 cm²	1
Wafer cost per unit area (M_2/A)	\$0.19/cm²	\$5.09/cm²	27
Wafer cost per unit area for 30% yield ($M_2/A/0.3$)	\$0.63/cm²	\$17/cm²	27

[a] Based on 1984 figures.
[b] Wafer thickness is 0.55 mm for Si and 0.75 mm for GaAs.

2. Fragile material: Since GaAs is a softer and more fragile material than Si, greater care must be exercised in GaAs wafer preparation. This results in substantially higher cost of wafer-shaping operations.
3. Higher density: GaAs has higher density (5.32 g/cm³ as compared to 2.33 g/cm³ for Si) and for a given diameter the GaAs wafer must be thicker than Si to avoid breakage. The cost of GaAs raw material required for a wafer is 40 times more than that for a Si wafer.
4. High vapor pressure: Unlike Si, which has a relatively low vapor pressure at its melting point (approximately 10^{-6} atm at 1412°C), both gallium and arsenic have much higher vapor pressures at the melting point of GaAs (10^{-4} and 1 atm, respectively, at 1238°C). To prevent decomposition of the melt during crystal growth, one has to make elaborate modification of the conventional Czochralski process (e.g., using a liquid encapsulation method). This also contributes to the higher cost per unit volume of GaAs ingot.

Referring to the bottom row of Table 1, the wafer cost (not yet processed) per unit area is \$0.63/cm² for Si and \$17/cm² for GaAs. The cost of bulk GaAs wafers is expected to remain an order of magnitude higher than Si in the foreseeable future. Therefore, in our view, a fundamental handicap of devices fabricated on bulk compound-semiconductor wafers is the cost of the material. It may appear that for a highly sophisticated chip almost any cost

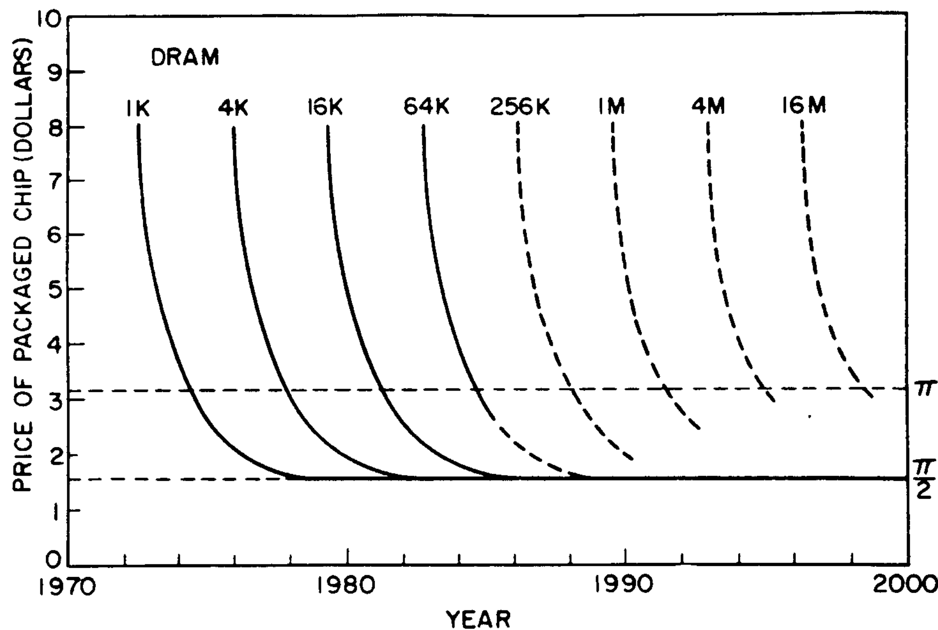

FIGURE 28. Pricing trends for Si integrated circuits illustrated by the average price of packaged dynamic random-access memory (DRAM) chips as a function of time in the past 14 years. (From Lepselter, M. and Sze, S. M., *IEEE Circuits Devices Mag.*, 1, 53, 1985. With permission.)

of the wafer can be justified by the added value of electronic circuitry. However, according to an empirical law,[129] for every more sophisticated chip, the initially high price decreases as its production technology matures, and it eventually settles at a price which is unacceptably low for replacement by III-V compound-semiconductor wafers. This law is illustrated in Figure 28 for dynamic random-access memories. As can be seen from the figure, the price of a packaged DRAM chip of any complexity drops over time to roughly the same level of less than \$2.00 per chip. Compared to that level, the \$17/cm^2 cost of GaAs wafers is prohibitively expensive. In our view, the cost consideration is likely to exclude from VLSI applications any ICs based on GaAs or InP bulk wafers.

From this conclusion (which we believe is shared by most of the experts in microelectronics), one often draws a vision of the future semiconductor industry in which there is a separation of markets between Si and III-IV compounds with different technologies catering to distinctive requirements. We believe, however, that such a coexistence of separate technologies can only be a temporary solution. In the long run (say, 10 years), this approach is not cost effective and it will yield to the emerging technology of monolithic hybrid material systems on low-cost Si substrates. Economic and technical advantages of such systems are self-evident. Their practical feasibility has become apparent in light of the recent dramatic developments in the field of silicon heteroepitaxy. These developments will be reviewed in the next section.

2. *Feasibility*

Until very recently, one could view the very possibility of obtaining device-quality GaAs layers on an Si substrate with a healthy skepticism, regarding it as a long shot at best. One could expect that a large lattice mismatch would necessarily result in a poor crystallinity of the epitaxial layer: large dislocation density, local strains, and grain boundaries. It was also

unclear whether the problem of antiphase disorder,* which has plagued the development of lattice-matched GaP on <100> Si devices, could ever be solved. Finally, one had to worry about the possible autodoping of the epilayers by Si atoms diffusing from the substrate.

This pessimistic outlook has been dramatically altered recently through the work of several research groups in the U.S. and Japan. Careful preparation of Si wafers (special cleaning procedures with subsequent thermal desorption under UHV conditions) enabled the investigators to grow epitaxial GaAs layers which were satisfactory for the fabrication of a number of devices with characteristics comparable to those obtained on bulk GaAs substrates. It turned out that the autodoping could be suppressed by a period of slow initial growth at reduced temperatures and that the antiphase domain boundaries could annihilate themselves in thicker layers. The lattice-mismatch problem is not specific to GaAs on Si; successful elimination of threading dislocations in epitaxial Ge on Si by the glitch-grading method discussed in Section III.A.1 may serve as a prototype solution. One may also use intermediate Ge layers, as some researchers have done; this makes good sense, since on the one hand, the lattice-mismatch between Ge and GaAs is only 0.13% and on the other hand, Ge grows well on Si (thus, one is able to treat the lattice-mismatch and the antiphase-domain problems in two separate steps). Whether or not intermediate Ge layers will become a part of the future technology is not clear, excellent results have already been obtained for devices manufactured in GaAs epitaxial layers on Si — both with and without Ge coating.

We shall not attempt to give a comprehensive review of all reported GaAs on Si heteroepitaxial devices. An incomplete list of most recent reports, which include MESFETs,[113,117-119] bipolar transistors,[122,123] double-heterostructure diode lasers,[115,125] and integrated GaAs-MODFET/Si-MOSFET circuits,[124] is sufficient to conclude that the feasibility of this approach is proven beyond doubt.

Ultimately, an assessment of the future GaAs/Si technology would have to include the cost of deposition. The MBE is inherently a slow-growth process not very suitable for deposition of thick layers. Commercial utilization of this technology will probably require another process capable of more rapid growth of thicker III-V compound layers, without introducing additional defects. A likely combination to emerge would involve a modified MOCVD reactor vacuum interlocked with a Si-MBE system, where UHV cleaning and possibly deposition of thin initial layers will take place. First reports of MOCVD growth of GaAs on <100>Si are quite encouraging.[116-118,120]

B. Heteroepitaxy of Semiconductors Other than GaAs

The general scope of incommensurate silicon heteroepitaxy includes the growth of a variety of materials, which can perform device functions unavailable in silicon. We have discussed the prototype examples of Ge and GaAs. One is obviously interested in other III-V and II-VI compound semiconductor systems on Si. However, growth on lattice-mismatched substrates generally results in misfit dislocations, which originate at the heterointerface and propagate up into the epitaxial layer. Both the electronic and optical properties of the working layers are degraded by these defects and effective schemes must be devised for their elimination.

At this time, the most promising method appears to be associated with trapping and deflection of dislocations by strained-layer superlattices (SLS).[11] We have described (Section III.A.1) an improvement of epitaxial Ge layers on Si by the glitch-grading method. Similar

* The formation of antiphase domains is a common problem encountered in the epitaxial growth of III-V compounds on nonpolar semiconductor substrates, such as Si or Ge. It represents an example of a broken symmetry in the nucleation of growth; both Ga and As can bond to a particular site on the substrate surface. The ambivalence is resolved in a different way in different parts of the sample, hence the formation of domains. One interesting approach to eliminating the antiphase disorder has been pursued by Kroemer and co-workers,[56] who proposed to use as substrates certain vicinal surfaces of silicon. They succeeded in growing single-domain GaP layers on <211> oriented silicon (see the discussion at the beginning of Section III).

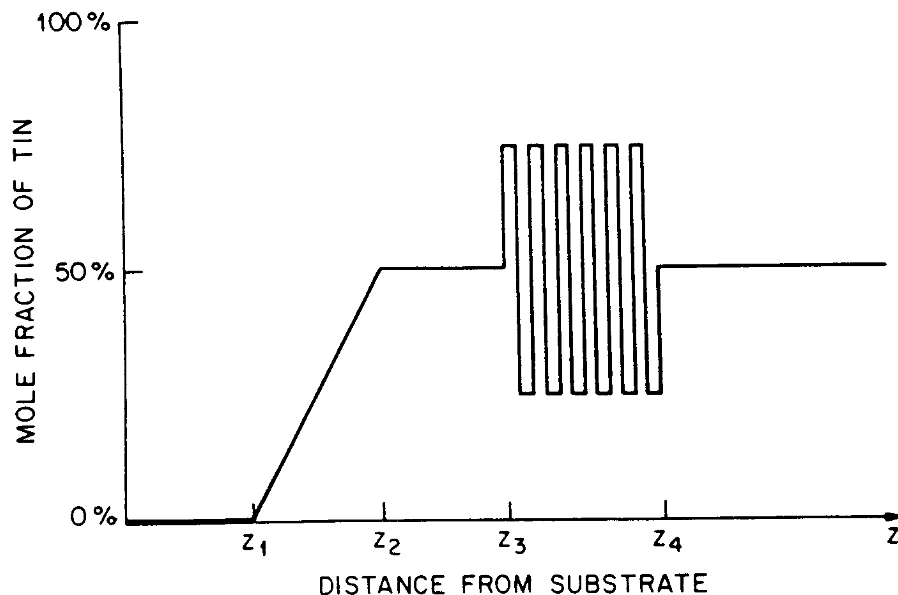

FIGURE 29. Proposed growth sequence for producing defect-free $Sn_{0.5}Si_{0.5}$ alloy. The alloy is preceded by a strained-layer superlattice of average composition equal to that of the alloy. The superlattice period (which is of order 10^{-6} cm) is exaggerated in the picture.

methods have been employed in the growth of lattice-mismatched GaAsP layers on GaP substrates and InGaAs layers on GaAs.[130] Two distinct strategies can be followed in the growth of device-quality compound-semiconductor layers on Si. One may try to improve the III-V layers above the interface by the MBE and MOCVD SLS techniques[130] developed for these materials. Alternatively, one may try to prepare the silicon substrate for subsequent lattice-matched growth. One such possibility is associated with the growth by Si-MBE of silicon/tin alloys, described in the next section. Another interesting, although not yet conclusively tested, approach consists in the possibility of dislocation-free growth of lattice-mismatched epitaxial layers on a porous or otherwise submicron-patterned silicon substrate.[72]

1. Metastable Alloys Si/Sn: Expanding Silicon Lattice

A recently proposed[131] variation of the SLS technique may be capable of preparing a silicon substrate for subsequent lattice-matched growth of a variety of semiconductors having a lattice constant larger than Si. The technique requires a low-temperature epitaxial growth, such as MBE, and consists of depositing tin/silicon alloys on Si substrates. One should in principle be able to grow dislocation-free Sn_xSi_{1-x} layers with any desired $x \leq 0.5$, i.e., with any lattice constant between 5.43 and $\approx$ 6 Å.

It is well known that unlike Ge/Si alloys which mix in any proportion, the Sn/Si alloys exhibit phase segregation when cooled from the melt. Because of this, there are no bulk solid alloys of silicon and tin. The problem of phase segregation does not arise, however, in a low-temperature epitaxy, which is a nonequilibrium process. One can expect a smooth growth of uniform Sn_xSi_{1-x} alloys on an appropriate lattice-matched substrate.

Starting from a silicon substrate, one can then use an adaptation of the SLS method for getting rid of misfit dislocations in the epitaxial alloy. This proposal[131] is conceptually quite similar to (and actually predates) the glitch-grading scheme, successfully used in growing high-quality Ge layers on Si for IR photodetector applications.[59] The required growth sequence to produce a $Sn_{0.5}Si_{0.5}$ alloy on a Si substrate is illustrated schematically in Figure 29. According to the idea of the SLS method,[11] misfit dislocations introduced during growth

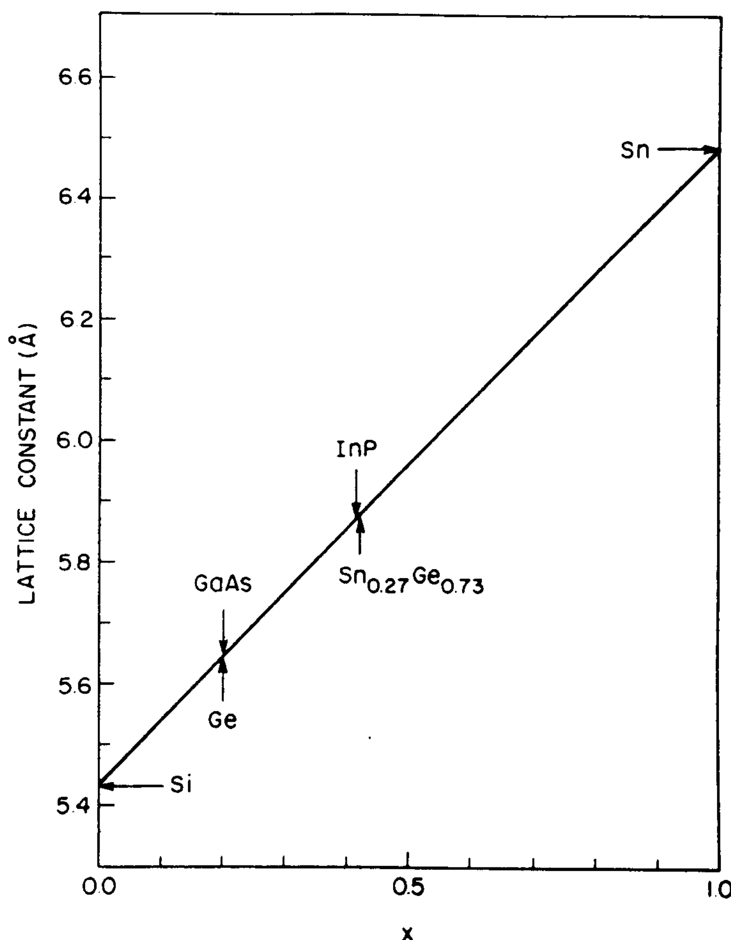

FIGURE 30. Lattice constants of Sn_xSi_{1-x} alloys.

of the graded layer $z_1 \rightarrow z_2$ will be trapped in the strained-layer region $z_3 \rightarrow z_4$, so that the alloy in the region $z > z_4$ is dislocation-free. It can be modified to grow a structure which terminates with a Sn_xSi_{1-x} layer with other values of x. The upper limit on x is determined by the thermal stability of the epitaxial layer at the temperature of growth and, possibly, the requirement of having a sufficient glitch amplitude above the average alloy composition. It is unlikely that the technique will be useful for $x > 0.5$.

The resultant alloy can be used as a substrate for growing other epitaxial materials of the same lattice constant. To appreciate the possible scope of the method, consider the plot in Figure 30, which shows the range of available lattice constants (assuming their linear interpolation). The lattice constants of selected semiconductors and the corresponding lattice-matched tin/silicon compositions are indicated by arrows. We see that GaAs and Ge lattices are accomodated by an Sn_xSi_{1-x} alloy with $x \approx 0.2$ and that even InP falls within $x \lesssim 0.5$ range.

2. Metastable Alloys Ge/Sn: Light from Column IV

We have also indicated in Figure 30 the position of a tin-germanium alloy Sn_xGe_{1-x} with $x = 0.27$. This alloy, which is lattice-matched with InP, is of considerable interest in its own right. On the basis of a theoretical model[132] for the band structure of gray tin, it was predicted[133,134] that the alloy Sn_xGe_{1-x} would have a direct bandgap for $x \gtrsim 0.25$. It should

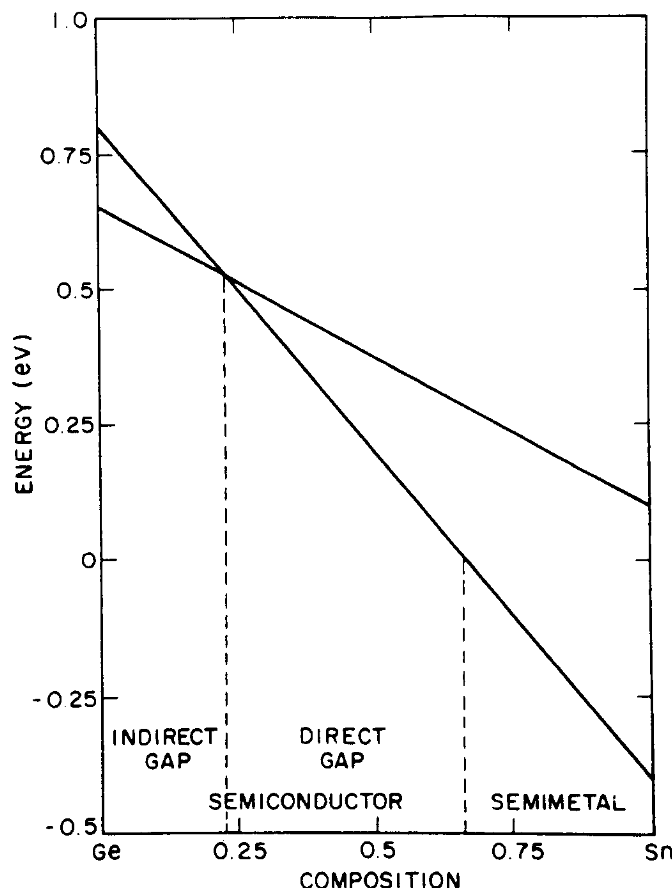

FIGURE 31. Predicted variation in the band-structure of tin-germanium alloys with increasing tin content. (From Oguz, S., Paul, W., Deutsch, T. F., Tsaur, B. -Y., and Murphy, D. V., *Appl. Phys. Lett.*, 43, 848, 1983. With permission.)

be remembered, of course, that like the Sn_xSi_{1-x} alloy, Sn_xGe_{1-x} does not exist in the equilibrium bulk form because of the phase segregation when the alloy is cooled from the melt. It can be expected, however, to grow epitaxially on the right substrate.[133,134] The positions of the conduction-band extrema in the alloy — relative to the top of the valence band — can be estimated by a linear interpolation of the known energies in the conduction bands of germanium and gray tin. Figure 31 shows the expected variation in the band structure of the Sn_xGe_{1-x} alloy as it goes over with increasing tin content x from an indirect-gap semiconductor to a semimetal. For $x \gtrsim 0.25$, the alloy will have the conduction band minimum in the Γ valley ($k = 0$) and therefore one can expect a high electron mobility and low effective mass. Even more significantly, this direct-gap material offers a unique possibility of fabricating long-wavelength ($\lambda \gtrsim 2.5$ μm) detectors, LEDs, and lasers using only Column IV elements. We conclude that the development of epitaxial (nonequilibrium) tin-silicon and tin-germanium alloys will add an important new dimension and tantalizing perspectives to the field of silicon heteroepitaxy.

C. The Future of Microelectronics: Hybrid Material Systems

In this section, we shall briefly discuss the most attractive potential uses of incommensurate Si heteroepitaxy. We are mainly concerned with VLSI applications, because "that's where

the money is". On the basis of the discussion above, we shall assume that all material problems associated with the epitaxial growth of device-quality heterolayers on <100> Si substrates will be solved in the not too distant future.

1. Special-Purpose Islands within Si-VLSI

We have relatively little doubt that Si will remain the basic VLSI material in any foreseeable future. Therefore, the most important applications will be those seeking to complement and enhance silicon technology rather than replace it altogether.

It has been convincingly argued[17] for the coexistence of the bipolar and CMOS technologies on a silicon chip. While CMOS is preferred for most internal logic gate elements, the bipolar is better suited for high-speed driving of high capacitance loads — long transmission lines and high fan-in nodes. These arguments can be extended to cover the emerging monolithically integrated heteroepitaxial technologies. As these technologies mature, they will enable the designer to replace the Si bipolar by GaAs heterojunction bipolar transistors, or MODFETs, or even some heterojunction hot-electron devices, to obtain even higher circuit speeds.

One can thus envisage a future chip architecture in which super high-speed GaAs/AlGaAs elements will be located on epitaxially grown islands on a silicon wafer, integrated with the Si circuits by a suitable metallization process. It is likely that the heteroepitaxial growth will take place after most of the silicon processing is done — except the metallization. Therefore, one should be concerned with the compatibility of the two technologies, although it appears to be a relatively minor issue at this point.

2. Intra- and Interchip Communications: Beacons on Silicon

At clock rates above several gigahertz, the on-chip interconnect lines represent a major problem in the VLSI technology. It can be expected to become even more severe in wafer-scale integrated circuits. In general, any interconnect line consisting of a metal runner on a dielectric or semiconducting surface can be modeled as an RCL transmission line with distributed resistances, capacitances, and inductances.[135] At high frequencies, this line becomes lossy leading to signal attenuation, which is moreover frequency dependent. The dispersion brings about a distortion of the signal waveform, which at best complicates the circuit design and at worst makes impossible the room-temperature operation of a large area VLSI at gigahertz clock rates. Furthermore, reactive coupling leads to a cross-talk between different lines. The inductive cross-talk (which is long range and thus couples even lines remote from each other) scales up with the increasing frequency and becomes dominant in the gigahertz range.[135]

All these problems can certainly be addressed within the conventional metallic-runner approach, e.g., by operating the circuits at reduced temperatures and designing special shields to eliminate the cross-talk.[136] Nevertheless there is, obviously, an enormous potential in the development of optical communications within a silicon wafer. There are many possible configurations for such a development with heteroepitaxial techniques. One may be able to use electronically triggered compound semiconductor lasers of light-emitting diodes of picosecond-pulse operation. Alternatively, one may use a constant light source and transmission modulators on the chip controlled by local silicon circuits. An interesting class of such electrooptic modulators can be based on two-dimensional room-temperature excitonic effects in quantum wells.[137] The optical signals can be sent to any part of the chip through virtually lossless dielectric ridge waveguides composed of, say, an amorphous Si core clad by two SiO_2 layers. At the receiving end, the signal will be processed by an IR detector on a special-purpose island integrated monolithically into the system. The light source for on-chip communications can itself be located outside the Si wafer; in a sense, it can be compared to a supply battery. The necessary on-chip elements will be light modulators, detectors, and waveguides (Figure 32).

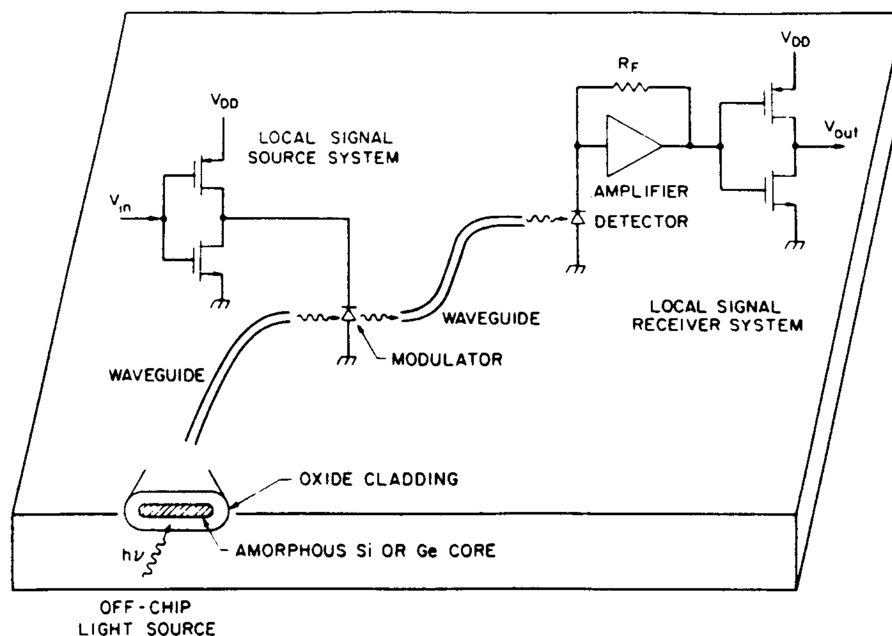

FIGURE 32. Illustration of the possible architecture for optical on-chip communications.

V. CONCLUSIONS

We have discussed a number of possible device applications of Si-MBE. However, we have not covered every direction of the present-day work. For example, we have left out any discussion of an important and classic subject of MBE research, the doping (*nipi*) superlattices, which had appeared in this paper only as silent ghosts in Figures 1 and 2. One reason for not going into this subject was furnished by the existence of an excellent review.[138] (Another reason is that the idea of doping superlattices is not at all specific to Si, so that most of the contemplated applications can be better realized in GaAs.) We have not done full justice either to the important topic of epitaxial insulators. Its potential for device applications can be expected to be greatly enhanced by further developments in the growth techniques, such as the deposition of both an insulator and a metal-silicide layer in one MBE growth sequence.[139]

Of the directions we have discussed, we are most enthusiastic about the prospects for device applications of heteroepitaxial materials on Si substrates, especially those we termed "incommensurate" (Section IV). We have argued our strongly held view that specialized heteroepitaxial islands within Si-VLSI wafers will become standard in the microelectronics of 1990s. This vision calls for the establishment of a radically new direction in semiconductor engineering, marked by the convergence of silicon and compound-semiconductor technologies rather than their separate developments.

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