VLSI Systems Design (ESE355)
Spring 2004; Instructor: Alex Doboli
Homework 2
Due on Monday, March 01 2004

Acknowledgement: This exercise was adapted after a homework idea by Prof. R. Vemuri, University of Cincinnati.

This homework introduces you to the design of layouts of basic digital circuits. You will use the MAGIC layout editor to draw your layout. For each of the layouts, extract the **.ext* file from the layout, convert it into **.sim* and **.spice* files using the ext2sim and ext2spice programs, and use IRSIM and HSPICE to verify your designs. You will further study the relationships between digital gate speed and layout parasitic.

Whereas you will learn the layout design rules as you go, it is a good idea that you go over the *SCMOS Design Rules* presented in the textbook.

For each of the following digital circuits, draw the layout and validate its functioning using IRSIM and HSPICE simulation. *In each case, try to achieve the most compact designs allowed by the design rules.* As you know, area minimization is an important design requirement for VLSI circuits. *In each layout, all inputs, outputs, and power wires must be brought out to the periphery of the bounding box.*

You will have to design following digital circuits:

1. ***CMOS inverter*** *whose rise and fall time are no ore than 0.2ns, when a 100fF external load is attached at its output terminal. The capacitive load is to be added by editing the *.sim file*
2. *A **2 input NAND gate** whose rise and fall times are no more than 0.2 ns, when a 100fF load is attached at its output terminal.*
3. *A **3-input NOR gate** whose rise and fall times are no more than 0.2ns, when a 100fF external load is attached at its output terminal.*
4. ***D master slave flip-flop**, which reliably operates at 100MHz clock frequency or higher when 100fF external loads are attached to the output terminals (at each Q and Q' terminals). As a starting point for the For D flip-flop schematics, use Figure 7.7 and Figure 7.10 in the textbook by J. Rabaey.*

For each design submit the following:

1. *The transistor level diagram with the W and L dimensions of each transistor marked.*
2. *A plot of the layout. On each plot write the bounding box area of the layout.*
3. *IRSIM and HSPICE waveforms indicating the simulation results.*
4. *For the 2 input NAND gate layout, estimate the propagation delays $t_{pH\text{-}L}$ and $t_{pL\text{-}H}$ using the analytical procedure discussed in class. How close are these values to the values obtained through IRSIM and HSPICE simulation. Discuss your results.*
5. *If the 4 gates are used as a basic cell library to implement larger digital circuits, what is the estimated clock frequency at which the larger digital circuits could operate? Discuss your opinion.*

Summarize what you have learned from these exercises. Your summary should be organized as a list of items and thumb rules, which you can use in the future.