**VLSI System Design (ESE 355)**
**Spring 2003; Alex Doboli**

**Home Work - 1**
**Due on Feb 10, 2003 (Monday)**

*Acknowledgement: This homework was developed by Prof. R. Vemuri, University of Cincinnati.*

This assignment has three purposes. First, to introduce you to switch-level simulation and the IRSIM switch level simulator. Second, to introduce you to the effects of transistor dimensions on the performance of VLSI designs. Third, to compare the accuracy of more detailed circuit simulators such as Spice with that of the switch level simulators.

Switch-level simulation is perhaps the most widely used form of simulation in the process of VLSI system design. Simulation at a higher level of abstraction, such as as the register transfer level and the gate level, while sufficient for functional aspects, may not model the circuit accurately enough to give a good idea about its performance. Simulation at a lower level of abstraction using detailed device models will give an accurate picture of the performance but is impractical in computation time for large circuits. Switch level simulators use simple linear models, consisting of voltage-controlled switches, resistors and capacitors, of the VLSI circuit to model both function and performance with reasonable accuracy. Switch level simulators are much faster than electrical simulators, such as Spice.

Switch level design represents the lowest level of functional abstraction to a VLSI mask layout. It retains all the function and performance-related attributes, viz. the transistors, their lengths and widths, their connectivity, the resistances and capacitances of various wires and nodes, while discarding the details of exact positioning of transistors and wires. A good VLSI designer should know switch-level design well.

In the following, assume minimum transistor dimensions of 2x2 microns. Rise time is the maximum time required to change a 0 at the output to a 1. Fall time is the maximum time required to change a 1 at the output to a 0.

1. *Switch Level Simulation:*

   (a) Implement a switch-level model of NOT, 2-input NAND and 2-input NOR gates. Using IRSIM, simulate the devices and make sure that they work correctly. *Submit the IRSIM source files and dumps of the analyzer windows showing the simulation results.*

(b) Attach a capacitor C to the output of each of the above gates. Change the value of C from 100 fF to 1000 fF in steps of 300 fF and simulate using IRSIM. For each gate, draw a graph with load capacitance on the x-axis and the rise-time and fall-time on the y-axis. *Submit the graphs.*

(c) Attach a 100 fF capacitor C to the output of the NOT gate. Keep the widths of the transistors at 2 microns and increase the lengths such that both the rise-time and fall-time become 5 ns. Increase C to 1000 fF in steps of 300 fF. In each case, manipulate the lengths and widths of the transistors such that the rise and fall times stay at 5 ns when measured using IRSIM. For each circuit, draw a graph with the capacitance on the x-axis and $W_n/L_n$ and $W_p/L_p$ on the y-axis. *Submit the graphs.*

(d) Attach a 500 fF capacitor to the output of the NAND and NOR gates. Adjust sizes of the transistors such that both the rise and fall times become 5 ns when measured using IRSIM. *Draw the circuits and note the values of W's and L's next to each transistor.*

2. *Detailed Device Level Simulation:*

   Spice is an electrical simulator that uses more detailed models of circuit components than IRSIM does.

   (a) Determine whether the sizing you have done for problem 1.d above is indeed accurate using Spice. That is, simulate the NAND and NOR gates you have designed using Spice. If the results show your sizing is inaccurate, resize the transistors such that the desired performance is demonstrated when simulated using Spice. *Submit various Spice generated waveforms with comments and the final transistor sizes if different from 1.d.*

*Summarize what you learned from these exercises. Your summary should be organized as a list of items and thumb rules which you can use in the future.*

What you should submit is shown in *italics*. Please don't submit anything less or more than what has been requested. Start early; the due date is firm.