VLSI System Design (ESE 355)
Spring 2003; Alex Doboli

Home Work - 2
Due on March 11, 2003 (Monday)

Acknowledgement: This homework was developed by Prof. R. Vemuri, University of Cincinnati.

This assignment introduces you to the design of layouts. You will use the Magic layout editor to draw the layouts. For each design, extract the **.ext* file from the layout, convert it into **.sim* and **.spice* files using the *ext2sim* and *ext2spice* programs, and use IRSIM and SPICE simulators to verify your designs.

Whereas you will learn the layout design rules as you go, it is a good idea to scan the *SCMOS Design Rules* I handed over in class.

For each of the following modules, draw the layout and validate its function using IRSIM/SPICE. *In each case, try to achieve the most compact designs allowed by the design rules.* In each layout, all the input, output and power wires must be brought out to the periphery of the bounding box.

For each design, submit (1) a transistor level diagram with the W and L dimensions of each transistor marked, (2) a plot of the layout, and (3) IRSIM/SPICE waveforms indicating the simulation results. Also, on each plot write the bounding box area of that layout.

1. Inverter whose rise and fall time are no more than 3 ns, when a 1pF external load is attached at the output terminal. The capacitive load is to be added by editing the **.sim* file.
2. 3-input NOR gate whose rise and fall times are no more than 5ns when a 1pF external load is attached to the output terminal.
3. D flip-flop which reliably operates at 10 MHz clock frequency or higher when 1pF external loads are attached to the output terminals (1pF at each Q and Q'). For D flip-flop schematics, use Figure 7.7 and Figure 7.10 in the textbook by J. Rabaey as starting points.

Summarize what you learned from these exercises. Your summary should be organized as a list of items and thumb rules which you can use in the future.