ESE 556: VLSI Physical and Logic Design Automation
Spring Semester 2003

Instructor: Alex Doboli, Ph.D.
Light Engineering Building, Room 261, Email: adoboli@ece.sunysb.edu

Schedule: Spring Semester 2003.

Goals: Upon completion of the course, students will know to design and implement *state-of the-art* CAD tools and algorithms for VLSI logic and physical level design. The discussed topics include physical (layout) specific tasks such as partitioning, floorplanning, module placement, and signal routing. Automated optimization of combinational and sequential circuits will be also presented. The course involves extensive project assignments.

Textbooks:

1) N. Sherwani, "*Algorithms for VLSI Physical Design Automation*", Kluwer, 1999.
2) G. Hachtel, F. Somenzi, "*Logic Synthesis and Verification Algorithms*", Kluwer, 1996.
3) Giovanni De Micheli, "*Synthesis and Optimization of Digital Circuits*", Mc-Graw Hill, 1994.
4) Published papers will be provided in class.

Prerequisites:

B.S. in Computer Engineering/Science or Electrical Engineering

Topics:

1) *Physical Design Automation*:

- Introduction to Design Automation and CAD Tools
- Basic Data Structures and Algorithms
- Logic and Circuit Partitioning
- Floorplanning and Placement
- Global and Detailed Routing

2) *Logic Design Automation*:

- Two-Level Combinational Logic Optimization
- Multiple-Level Logic Optimization
- Sequential Logic Optimization
- Cell-Library Binding
- Integrated Logic and Physical Design Automation

Assignment Schedule and Grading:

Project 1 (*Physical Design Automation*: Partitioning, Floorplanning)	10%
Project 2 (*Physical Design Automation*: Placement, Routing)	20%
Project 3 (*Logic Design Automation*: Library Binding, Two/Multiple Level Logic Minimization)	20%
Midterm	20%
Final	30%