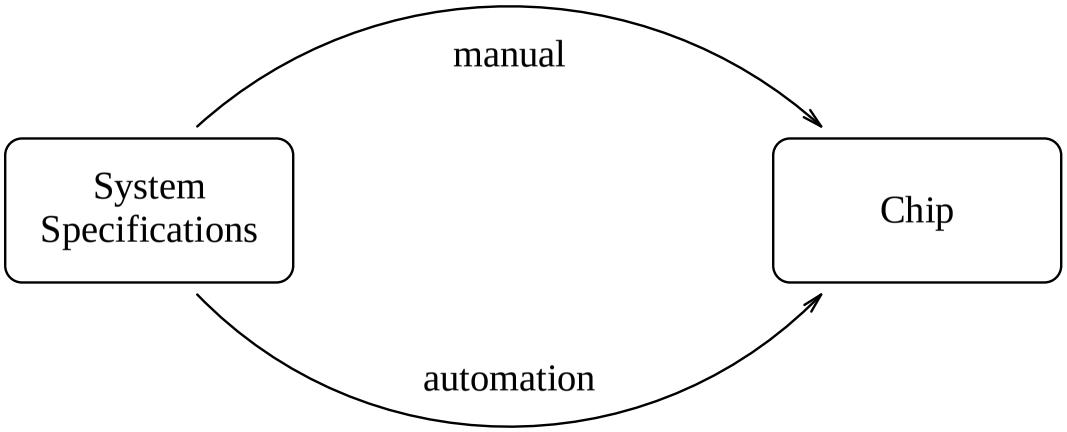
VLSI Physical Design Automation

Objectives:

- Obtain a general understanding of IC's.
- Study the basic algorithms used in designing the layout of a chip.
- Study algorithms which convert a circuit description into a geometric description.
- Study the differences in algorithms that perform the same operations.

VLSI Design Cylce

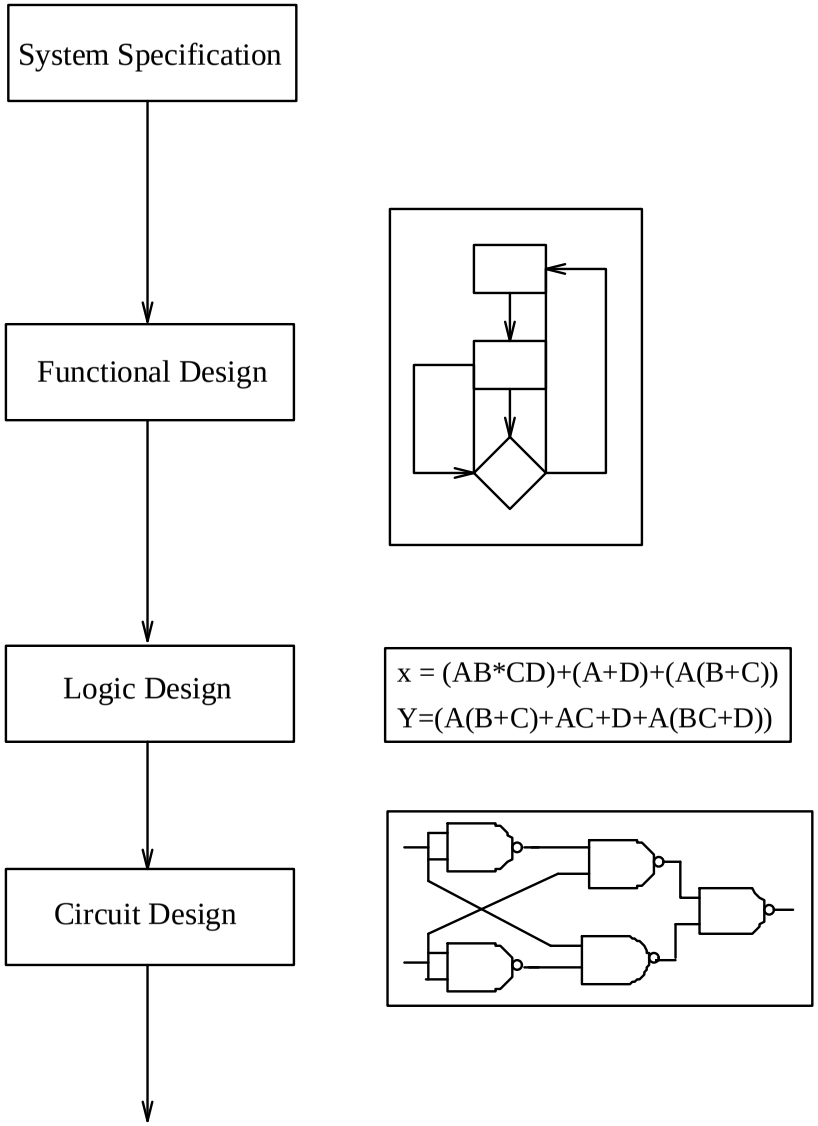


- Large number of devices
- Optimization requirements for high performance
- Time-to-market competition
- Cost

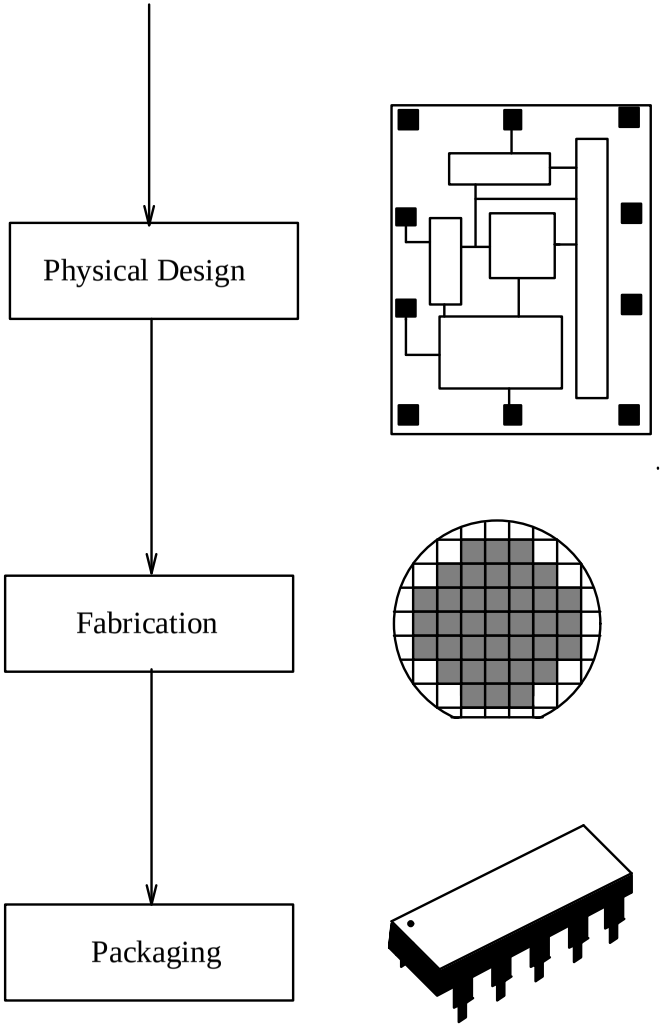
VLSI Design Cycle

1. System Specification
2. Functional Design
3. Logic Design
4. Circuit Design
5. **Physical Design**
6. Design Verification
7. Fabrication
8. Packaging, Testing, and Debugging

VLSI Design Cycle



VLSI Design Cycle (cont.)

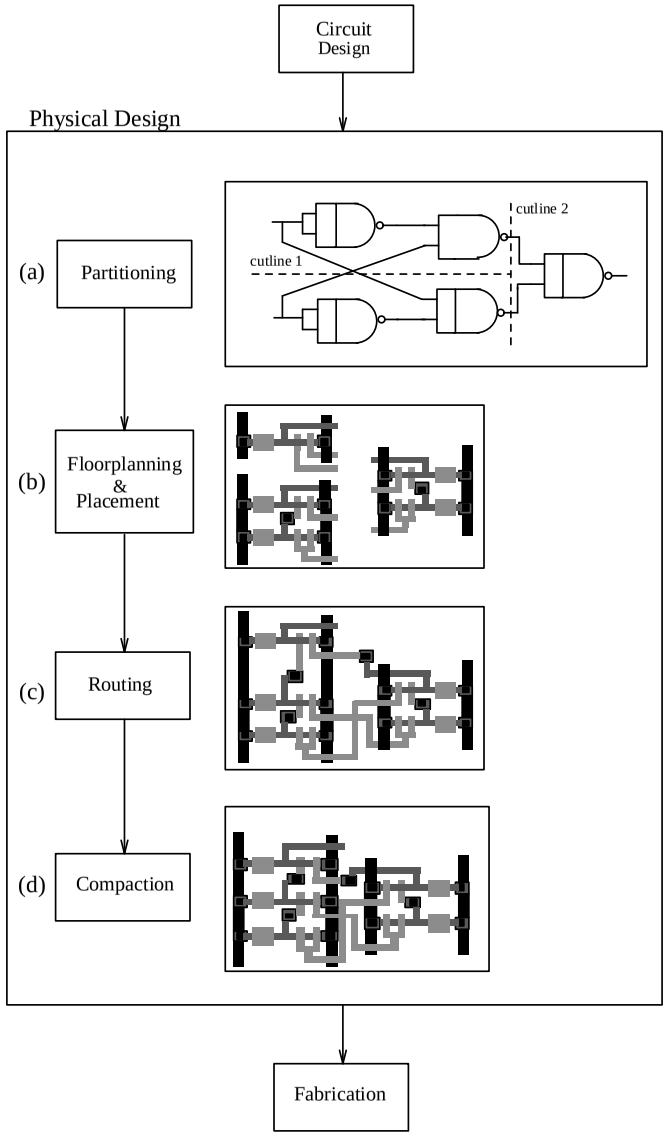


Physical Design

Physical design converts a circuit description into a geometric description. This description is used to manufacture a chip. The physical design cycle consists of

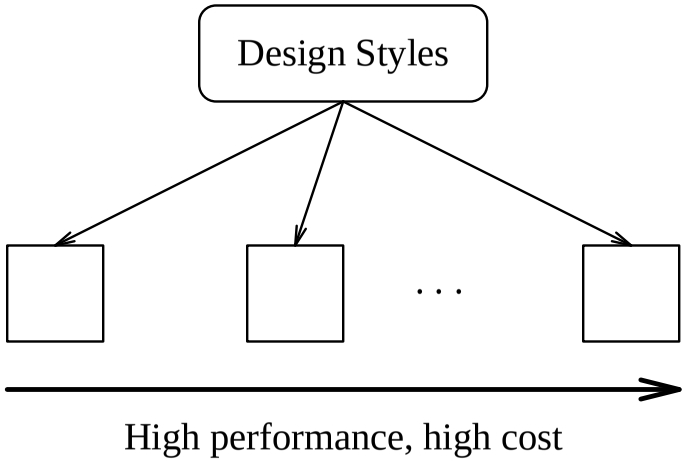
1. Partitioning
2. Floorplanning and Placement
3. Routing
4. Compaction

Physical Design Cycle

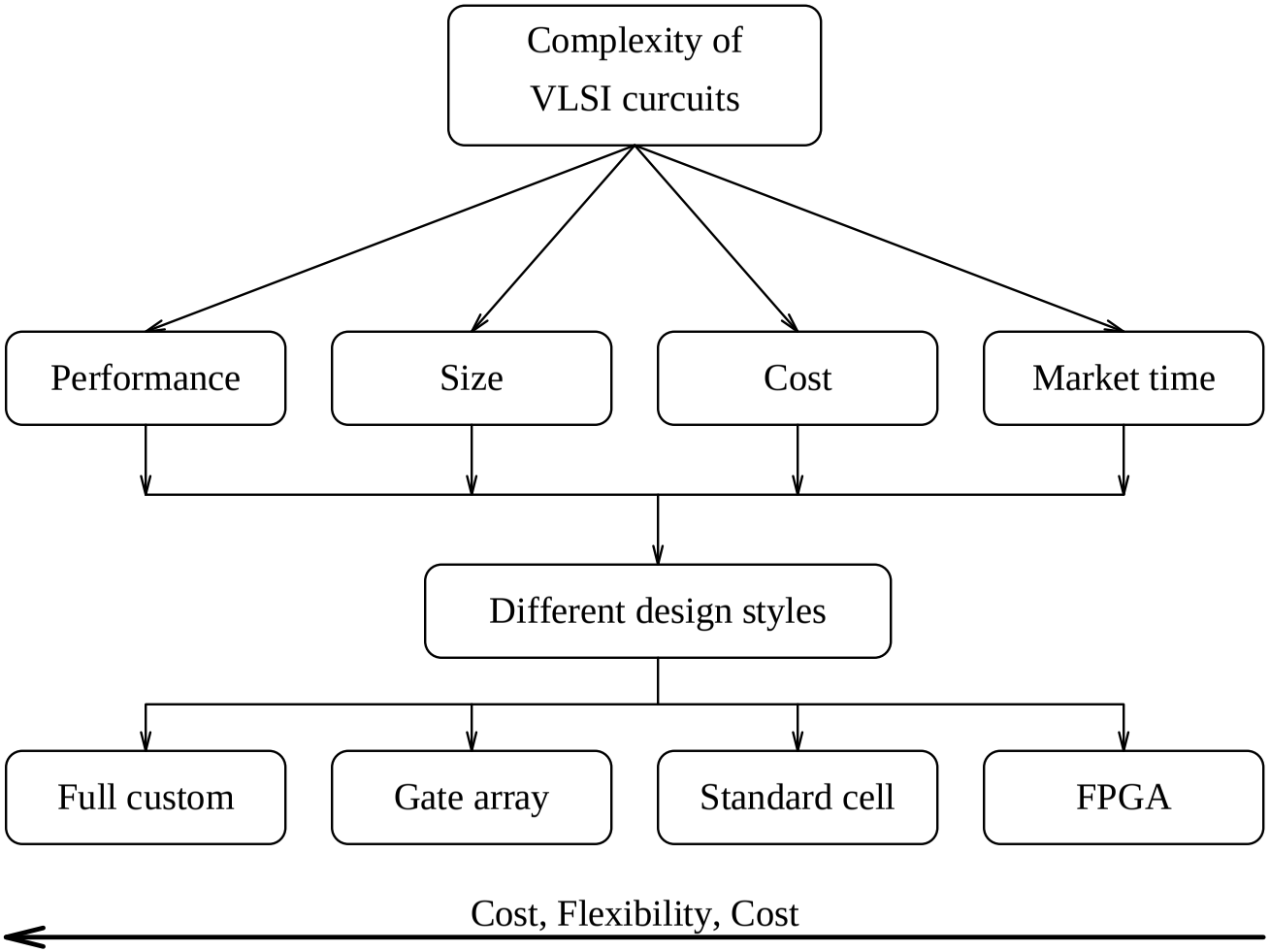


Complexities of Physical Design

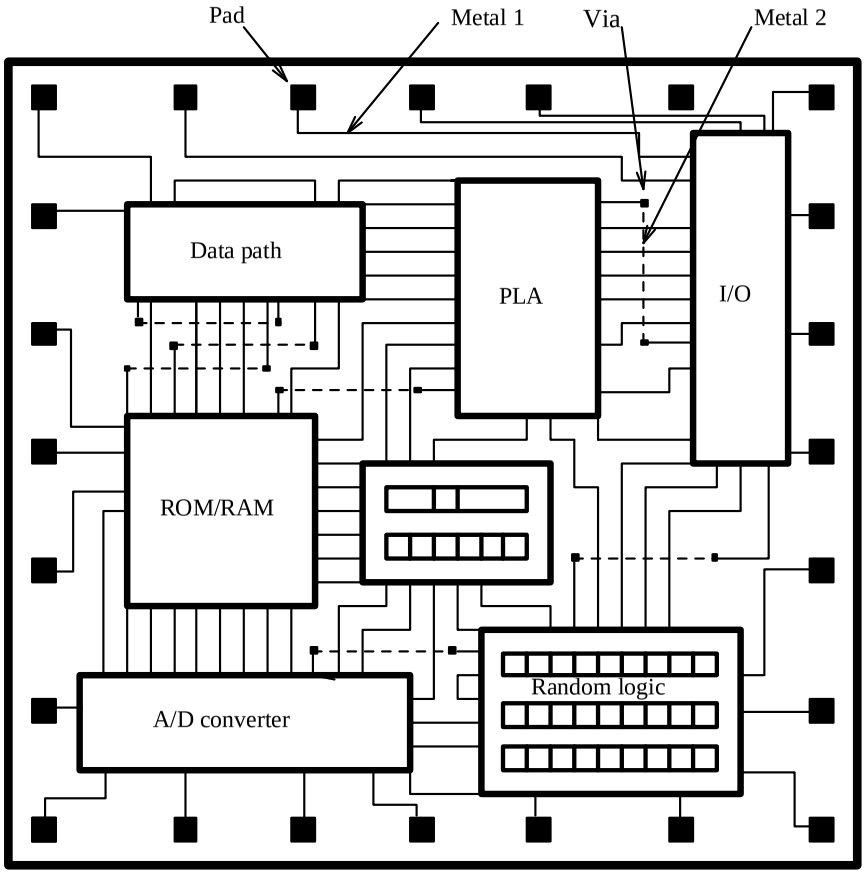
- More than 3 million transistors
- Performance driven designs
- Time-to-market



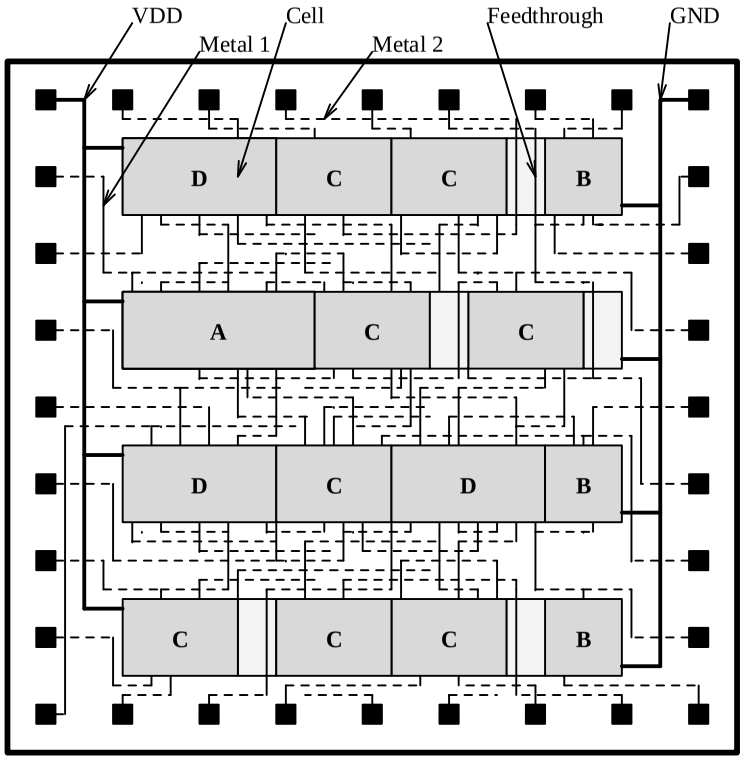
Design Styles

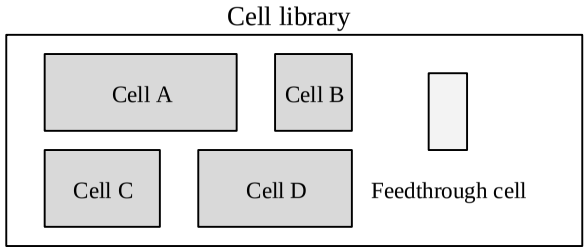


Full Custom Design Style

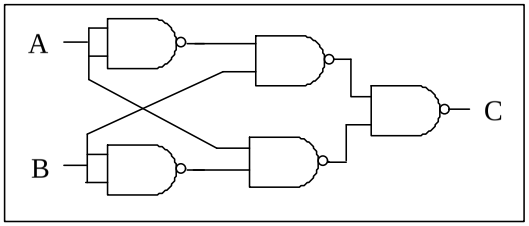


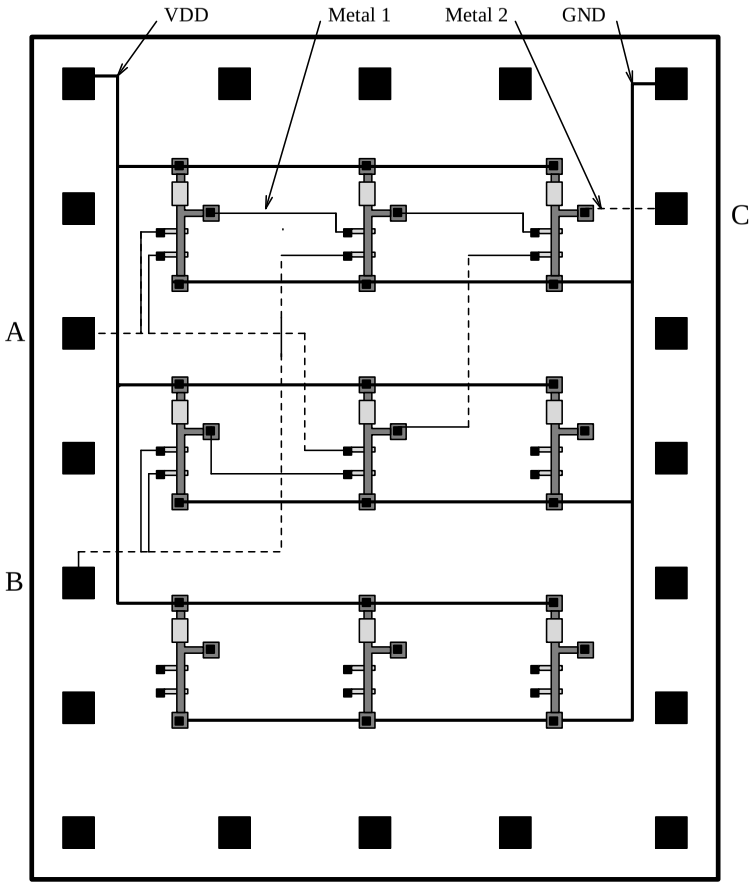
Standard Cell Design Style



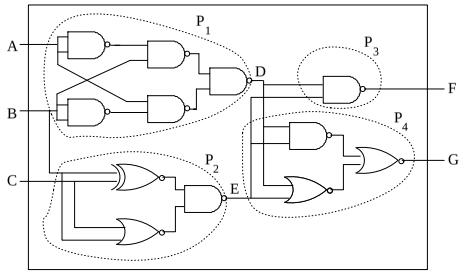


Gate Array Design Style





FPGA Design Style



(a)

P1

A	B	D
0	0	0
0	1	1
1	0	1
1	1	0

P2

B	C	E
0	0	0
0	1	1
1	0	1
1	1	1

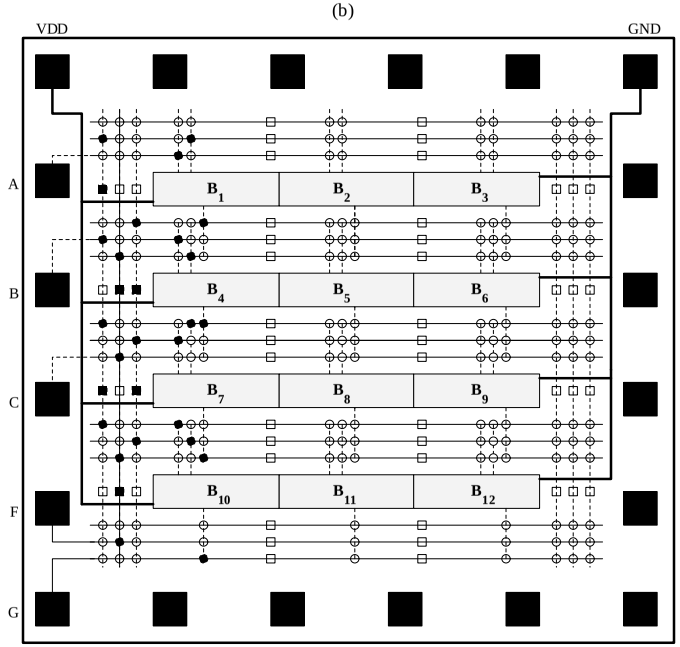
P3

D	E	F
0	0	1
0	1	1
1	0	1
1	1	0

P4

D	E	G
0	0	0
0	1	0
1	0	0
1	1	1

(b)



(c)

Comparisons of Design Styles

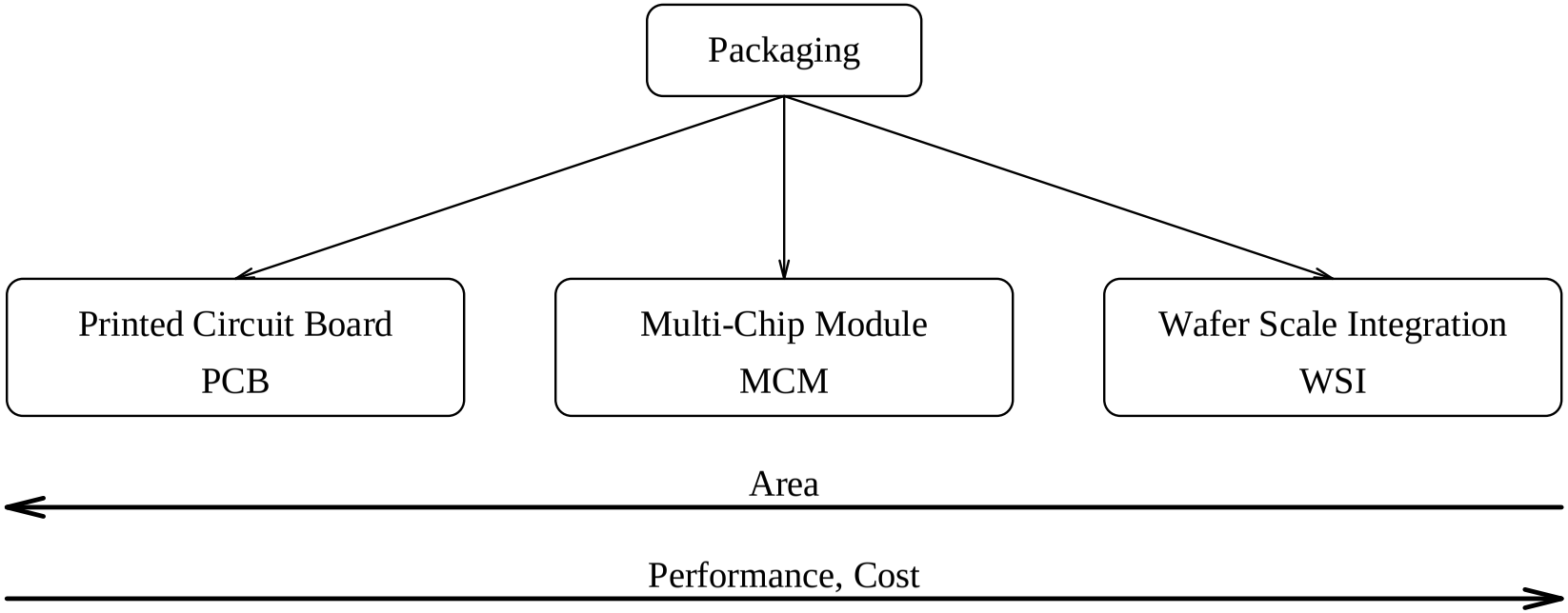
	style			
	full-custom	standard cell	gate array	FPGA
cell size	variable	fixed height*	fixed	fixed
cell type	variable	variable	fixed	programmable
cell placement	variable	in row	fixed	fixed
interconnections	variable	variable	variable	programmable

* uneven height cells are also used.

Comparisons of Design Styles

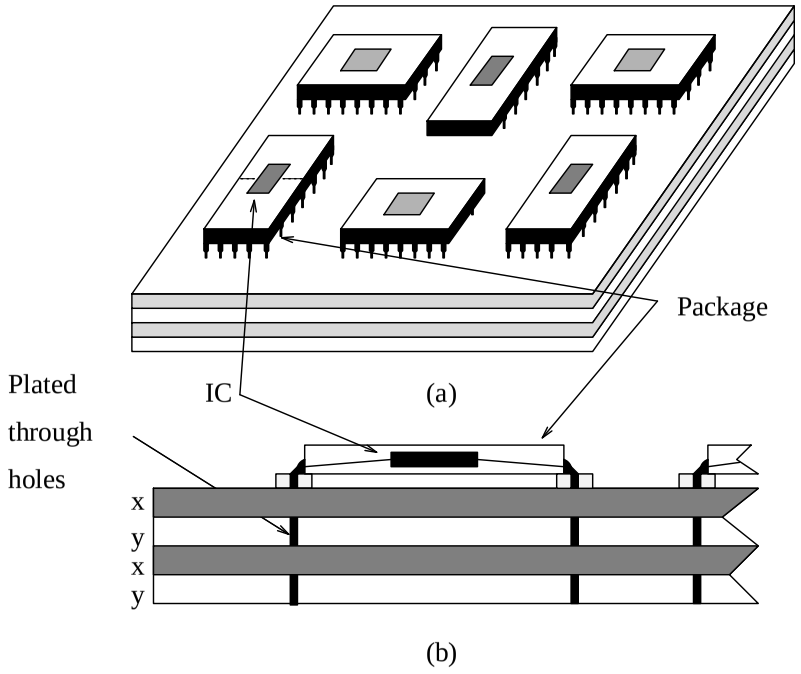
	style			
	full-custom	standard cell	gate array	FPGA
Area	compact	compact to moderate	moderate	large
Performance	high	high to moderate	moderate	low
Fabrication layers	All	All	routing layers	none

Packaging Styles



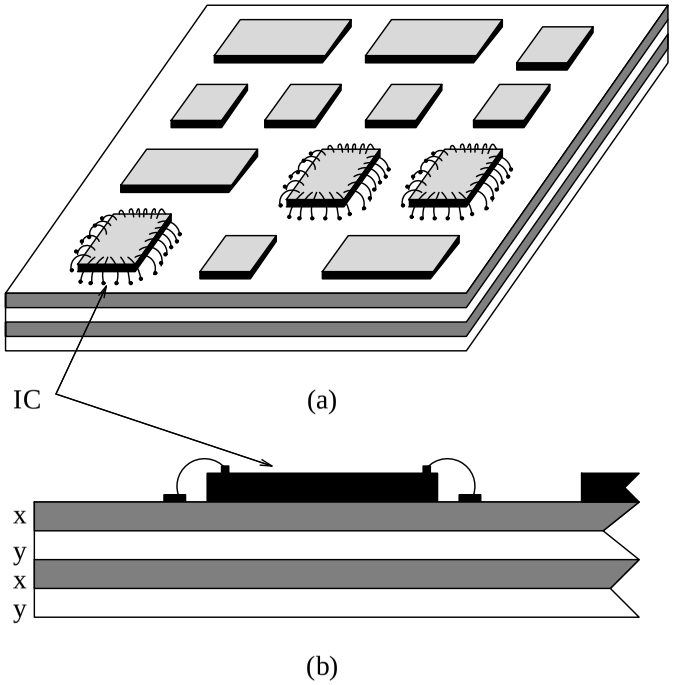
The increasing complexity and density of the semiconductor devices are driving the development of more advanced VLSI packaging and interconnection approaches.

Printed Circuit Board Model



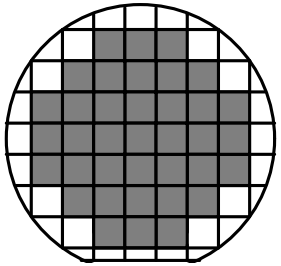
- Large number of layers (150λ pitch)
- Large area
- Low performance
- Low cost

MCM Model



- Up to 36 layers (75λ pitch)
- Moderate to small area
- Moderate to high performance
- High cost
- Heat dissipation problems

Wafer Scale Integration



- Small number of layers (VLSI technology - 6λ pitch)
- Smallest area
- Significant yield problems
- Very High performance
- Significant heat dissipation problems

Comparisons of Packaging styles

Technology	Figure of Merit (inches/psec . density inches/sq in)
WSI	28.0
MCM	14.6
PCB	2.2

History of VLSI CAD

Year	Design Tools
1950-1965	Manual design
1965-1975	Layout editors Automatic routers (for PCB) Efficient partitioning algorithm
1975-1985	Automatic placement tools Well defined phases of design of circuits Significant theoretical development in all phases
1985-present	Performance driven placement and routing tools Parallel algorithms for physical design Significant development in underlying graph theory Combinatorial optimization problems for layout

VLSI CAD Conferences

- ACM/IEEE Design Automation Conference (DAC)
- International Conference on Computer Aided Design (ICCAD)
- IEEE International Symposium on Circuits and Systems (ISCAS)
- International Conference on Computer Design (ICCD)
- IEEE Midwest Symposium on Circuits and Systems (MSCAS)
- IEEE Great Lakes Symposium on VLSI (GLSVLSI)
- European Design Automation Conference (EDAC)
- International Conference on VLSI Design

VLSI CAD Journals

- IEEE Transactions on CAD of Circuits and Systems
- Integration
- Transactions on Circuits and Systems
- Journal of Circuits, Systems and Computers
- Algorithmica
- SIAM journal of Discrete and Applied Mathematics
- IEEE Transactions on Computers

VLSI CAD Organizations

- ACM SIGDA
- Design Automation Technical Committee (DATC)

  of IEEE Computer Society

Summary

1. Physical design is one of the steps in the VLSI design cycle.
2. Physical design is further divided into partitioning, placement, routing and compaction.
3. There are five major design styles, e.g., full custom, standard cell, gate array, sea of gates and FPGAs.
4. There are three alternatives for packaging of chips, e.g., PCB, MCM and WSI.
5. Automation reduces cost, increases chip density, reduces time-to-market, and improves performance.
6. CAD tools currently lag behind fabrication technology, which is hindering the progress of IC technology.