Placement, Floorplanning and Pin Assignment

Partitioning leads to :

- Blocks with well defined areas and shapes (Fixed blocks)
- Blocks with approximated areas and no particular shape (Flexible blocks)
- A netlist specifying connections between the blocks

Objectives:

- Find locations for all blocks
- Shapes of flexible blocks
- Pin locations for all the blocks

Placement

Input to the placement problem:

- A set of blocks with well defined shapes
- Pin locations
- A netlist

Objectives:

- Minimize area
- Reduce netlength for critical nets

Floorplanning

Input to the floorplanning problem:

- A set of blocks, both fixed and flexible
- Pin locations of fixed blocks
- A netlist

Objectives:

- Minimize area
- Determine shapes of flexible blocks
- Reduce netlength for critical nets

Pin Assignment

Input to the Pin assignment problem:

- A placement of blocks
- Number of pins on each block, possibly an ordering
- A netlist

Objectives:

- To determine the pin locations on the blocks to reduce netlength

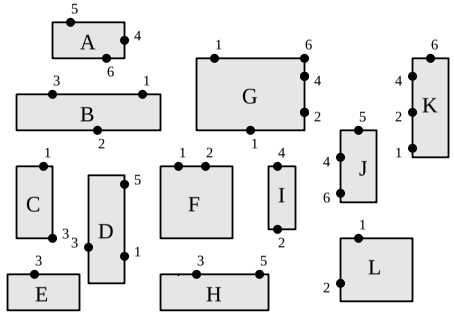
Factors to be considered

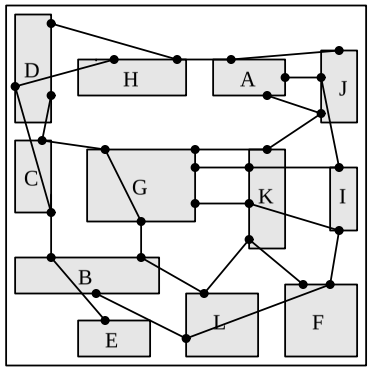
1. Shape of the blocks
2. Routing considerations
3. Placement for high performance circuits
4. Packaging considerations
5. Pre-placed blocks

Placement problems at different levels

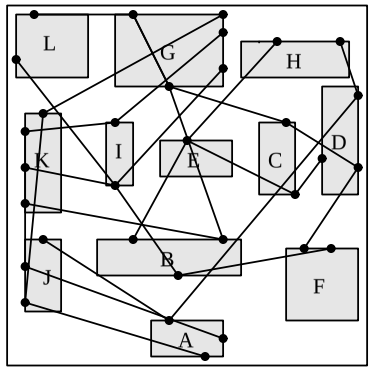
1. System level placement
   - Area
   - Heat dissipation
2. Board level placement
   - Fixed area available
   - Some chips may be preplaced
   - Minimize routing layers
   - Heat dissipation
3. Chip level placement
   - Limited number of layers
   - Minimum area

Consequences of Placment





(a)



(b)

Placement Problem Formulation

1. No two rectangles overlap, that is,

   $R_i \cap R_j = \phi$, $1 \leq i, j \leq n$.

2. Placement is routable, that is,

   $Q_j, 1 \leq j \leq k$, is sufficient to route all the nets.

3. The total area of the rectangle bounding

   $\mathcal{R}$ and $\mathcal{Q}$ is minimized.

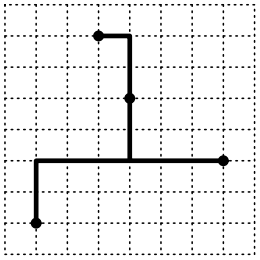
4. The total wirelength is minimized, that is,

   $\Sigma_{i=1}^{m} L_i$ is minimized.

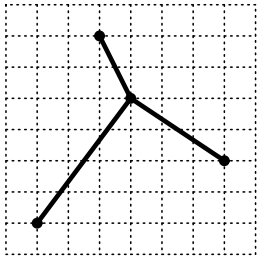
5. In the case of high performance circuits,

   the length of longest net $\max\{L_i \mid i = 1, \ldots, m\}$ is minimized.

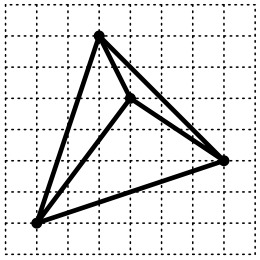
Interconnection Net Topologies in Placement Problems



(a) Steiner tree
(length = 13)



(b) minimum spanning tree
(length = 15)



(c) complete graph
(length = 32)

- Steiner trees
- Minimum Spanning Trees
- Complete graphs

Classification of Placement Algorithms

1. Simulation based algorithms
   (a) simulated annealing
   (b) simulated evolution
   (c) force directed placement
2. partitioning based algorithms
   (a) Breuer's Algorithm
   (b) Terminal Propagation Algorithm
3. Other Placement Algorithms
   (a) Cluster Growth
   (b) Quadratic Assignment
   (c) Resistive Network Optimization
   (d) Branch-and-Bound Technique
4. Performance Driven Placement

Simulated Annealing

- Simulation of the annealing process used to temper metals
- Avoids getting trapped in local minimums
- Initial placement available
- Improvements made to initial placement by exchanging blocks
- Moves which decrease cost are accepted directly
- Moves which increase cost are accepted depending on parameter T

Simulated Annealing Algorithm

Algorithm SIMULATED-ANNEALING
begin
    $temp$ = INIT-TEMP;
    $place$ = INIT-PLACEMENT;
    while ($temp >$ FINAL-TEMP) **do**
        while ($inner\_loop\_criterion$ = FALSE) **do**
            new_place = PERTURB($place$);
            ΔC = COST(new_place) - COST($place$);
            if ($\Delta C < 0$) **then**
                $place = new\_place$;
            else if (RANDOM$(0,1) > e^{\frac{\Delta C}{T}}$) **then**
                $place = new\_place$;
        $temp$ = SCHEDULE($temp$);
end.

Breuer's Algorithm

Partitioning technique used to generate a placement

A circuit is partitioned repeatedly by alternate horizontal and vertical cut lines

The available layout area is also partitioned identically

Till each subcircuit consists of a single gate and has a unique place on the layout area.

1. Objectives functions:
2. Total net-cut objective function
3. Min-max cut value objective function

   Sequential cut line objective function

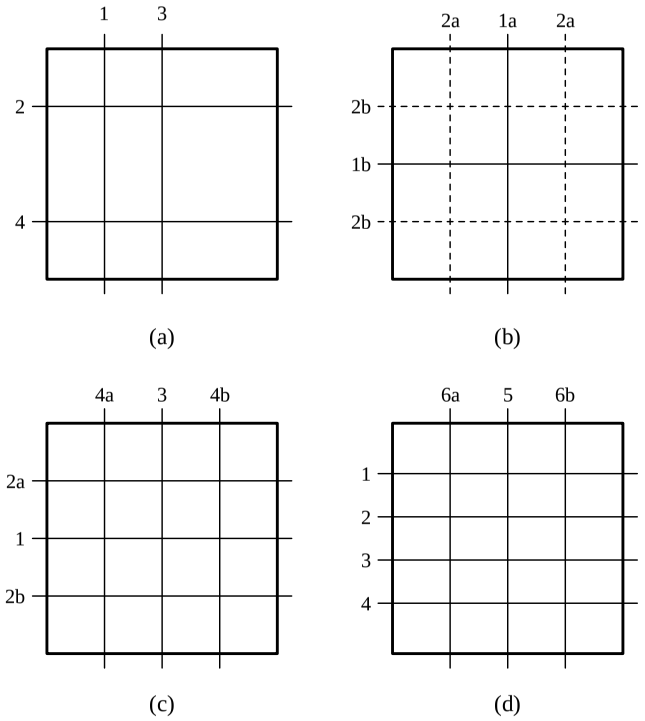
Different Sequence of Cut Lines Used in Breuer's Algorithm

a. Cut Oriented Min-Cut Placement

b. Quadrature Placement Procedure

c. Bisection Placement Procedure

d. Slice Bisection Placement Procedure



Floorplanning Algorithms

Classification

- Constraint based methods
- Integer programming based methods
- Rectangular dualization based methods

Constraint based floorplanning

Generate horizontal and vertical constraint graphs

Identification of critical paths

Remove redundant constraints from critical paths

Only improved floorplans are stored

Integer Programming based floorplanning

Use of linear equations using 0/1 integer variables

Two types of constraints considered:

- Overlap constraints
- Routability constraints

Pin Assignment

Summary

1. Placement and floorplanning are key steps in physical design cycle.
2. Floorplanning is the super problem of placement, since in addition to finding the location of blocks, it finds appropriate shapes for each block.
3. The pin assignment is usually carried out after the blocks have been placed to reduce the complexity of the overall problem.
4. Simulated annealing and simulated evolution are two most successful placement algorithm.
5. Integer programming based algorithms for floorplanning have been also been successful.
6. The output of the placement phase must be routable, otherwise placement has to be repeated.