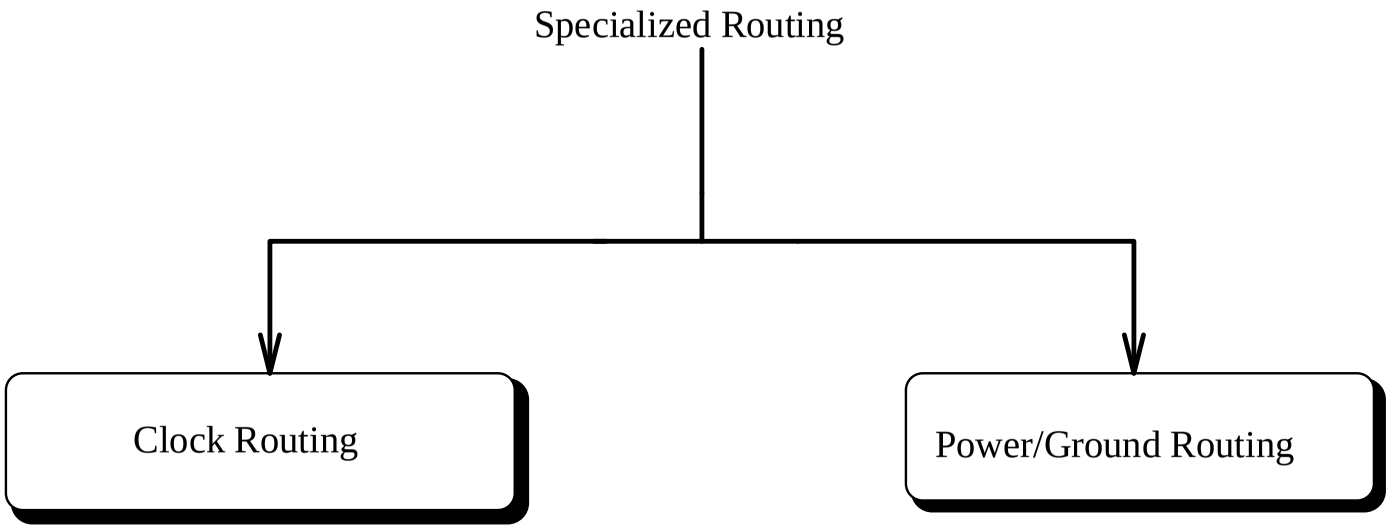
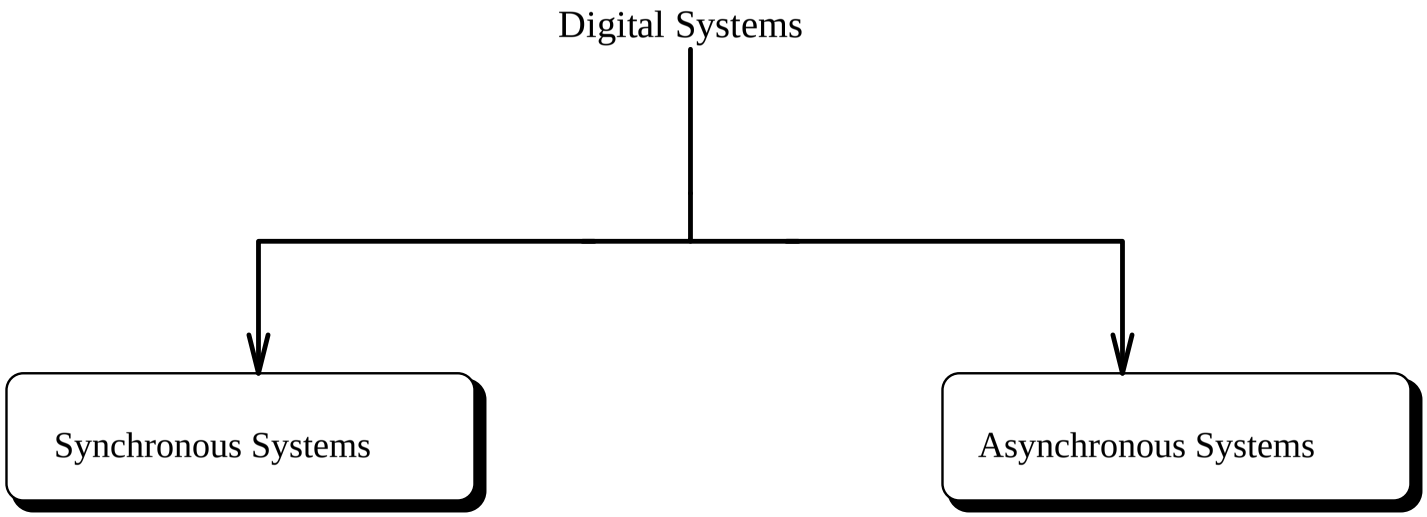
Specialized Routing



- Routing clock nets such that
  - clock arrives simultaneously
  - clock delay is minimum

- Routing of power/ground net on
  - Low resistance metal lines

Digital Systems

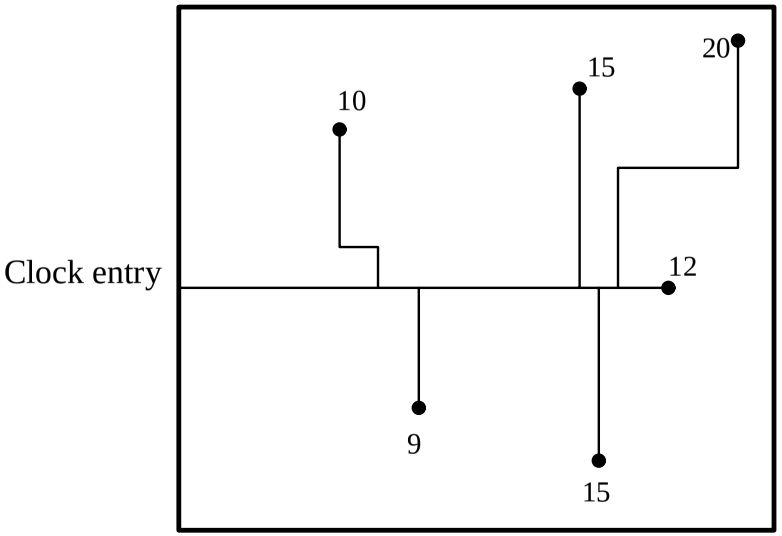


- Highly precised Clock achieves Communication and timing

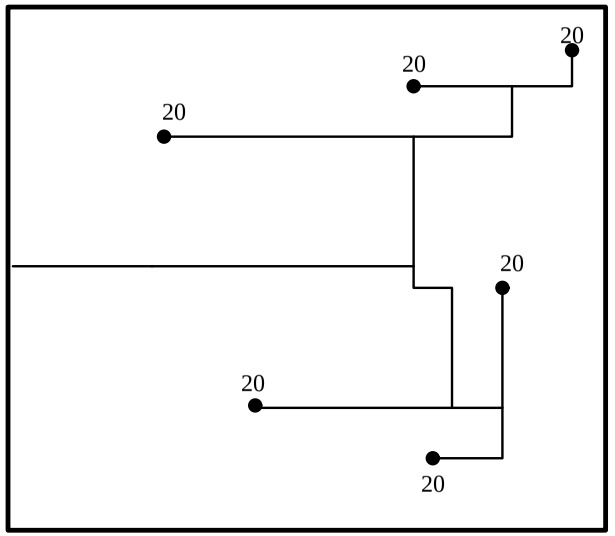
- Handshake protocol achieves the timing requirements of the system.

Clock Skew

Clock skew is defined as the difference in the minimum and the maximum arrival time of the clock.



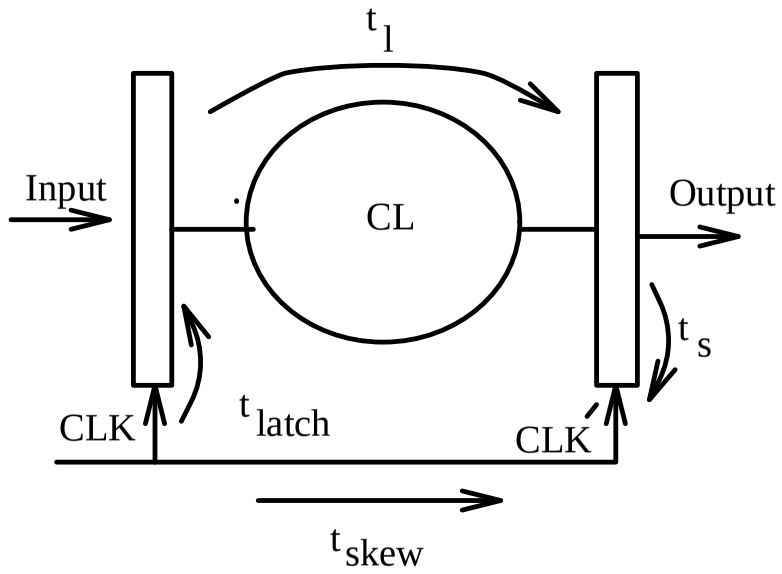
Clock skew = 20 - 9 = 11 units



Clock skew = 0

Clocking Schemes

Single Phase



$$t_{cp} > t_{latch} + t_l + t_s + t_{skew}$$

where

t_{latch} = Latch Delay

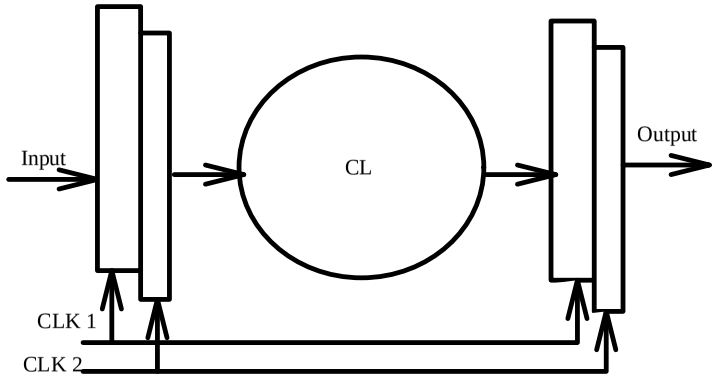
t_l= Delay through a logic block

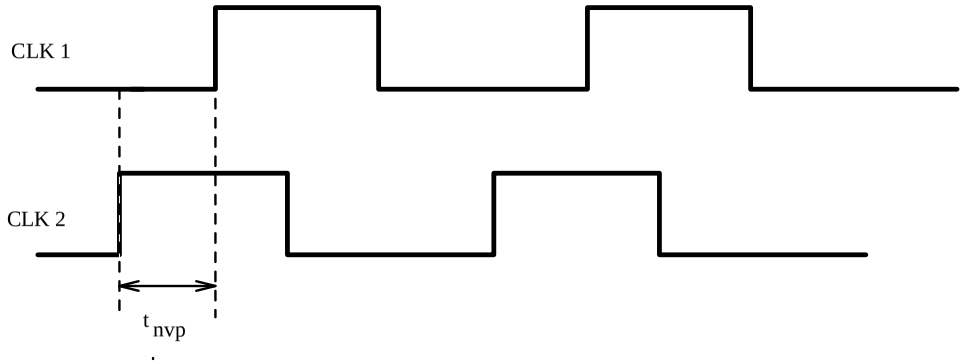
t_s= Set-up time

t_{skew}= Worst case skew between clocks.

Clocking Schemes (contd.)

Two Phase





$$t_{cp} > t_{nvp} + t_l + t_s + t_{skew}$$

where, t_{nvp} is non-overlapping time between two clocks.

Design Considerations of the Clocking System

1. Length of the longest clock net.

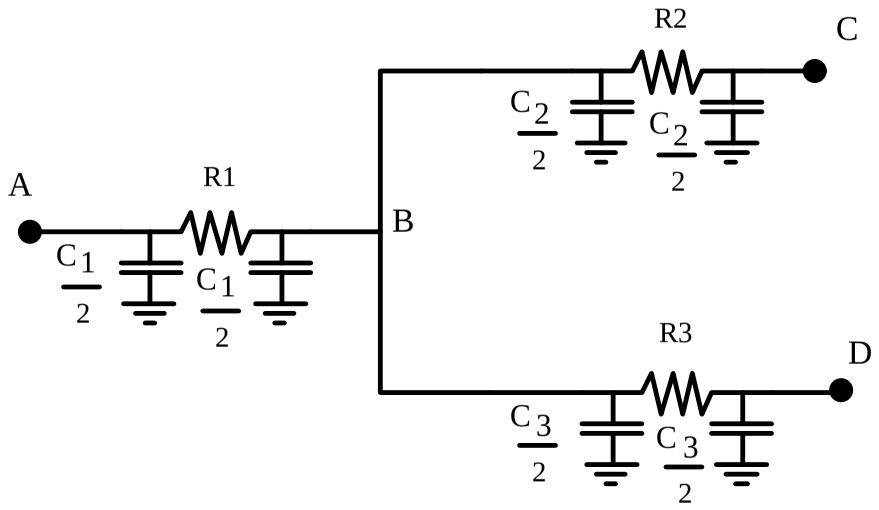
2. The delay caused by long wires is due to their capacitance and resistance. The delay is called the RC delay.

3. RC delay increases as the square of the scaling factor.

4. RC delay can be reduced by the use of buffers (repeaters), which also help to preserve the clock waveform.

5. The buffers, however, have internal delays, which must be taken into account when computing the total delay.

Delay Calculation for the Clock Tree



The RC delay from A to B is

$D_{AB} = R_1(\frac{C_1}{2} + C_2 + C_3)$

The delay from B to C is

$D_{BC} = R_2(\frac{C_2}{2})$

Similarly,

$D_{BD} = R_3(\frac{C_3}{2})$

Delay Calculation (contd.)

In general, the equivalent subtree capacitance at node i
is given as

$$C_i = \begin{cases} c_i & \text{If node } i \text{ is a buffered node} \\ c_i + \Sigma_{j \in IS(i)} C_j & \text{Otherwise} \end{cases}$$

Where c_i is the capacitance of node i and C_j
is the capacitance of all immediate successors of node i.

Objectives of Clock Routing

- Reduced Cock Skew:

  Reduced clock skew improves circuit performance.

- Less Delay:

  Less delay guarantees faster clocks (high frequencey).

Clock Routing Problem

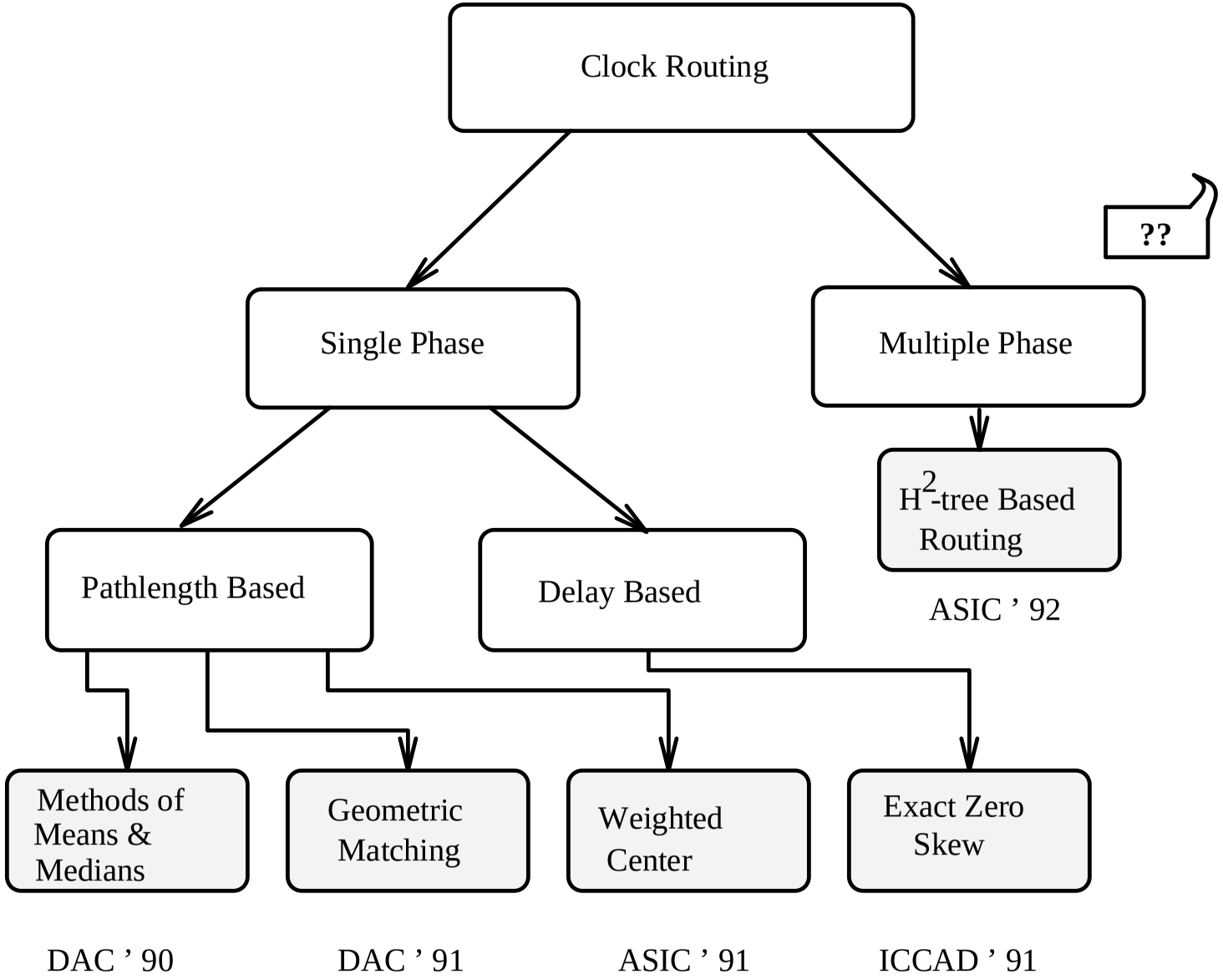
Given the routing plane and a set of points $\mathcal{P} = \{P_1, P_2, \ldots, P_n\}$ within the plane and clock entry point P_0 on the boundary of the plane, then the Clock Routing Problem(CRP) is to interconnect each $P_i \in \mathcal{P}$ such that:

$$\max_{i \in \mathcal{P}} t(0, i)$$

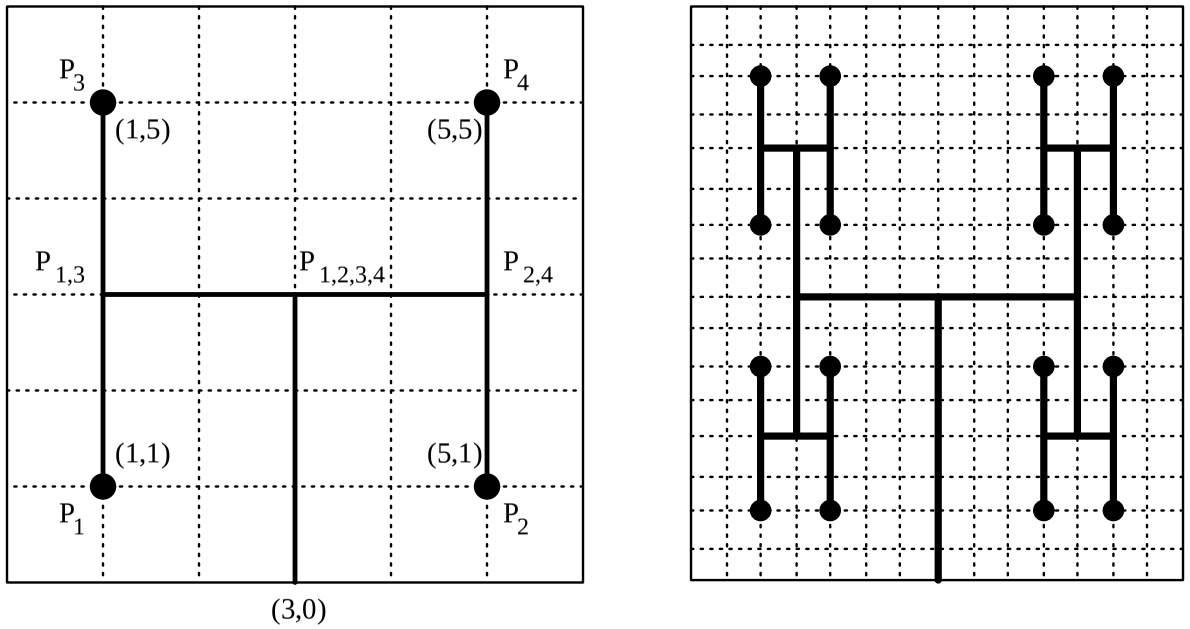
$$\max_{(i,j) \in \mathcal{P}} \mid t(0, i) - t(0, j) \mid$$

are both minimized.

Clock Routing Algorithms



H-tree Based Algorithm



(a) H-tree over 4 points (b) H-tree over 16 points

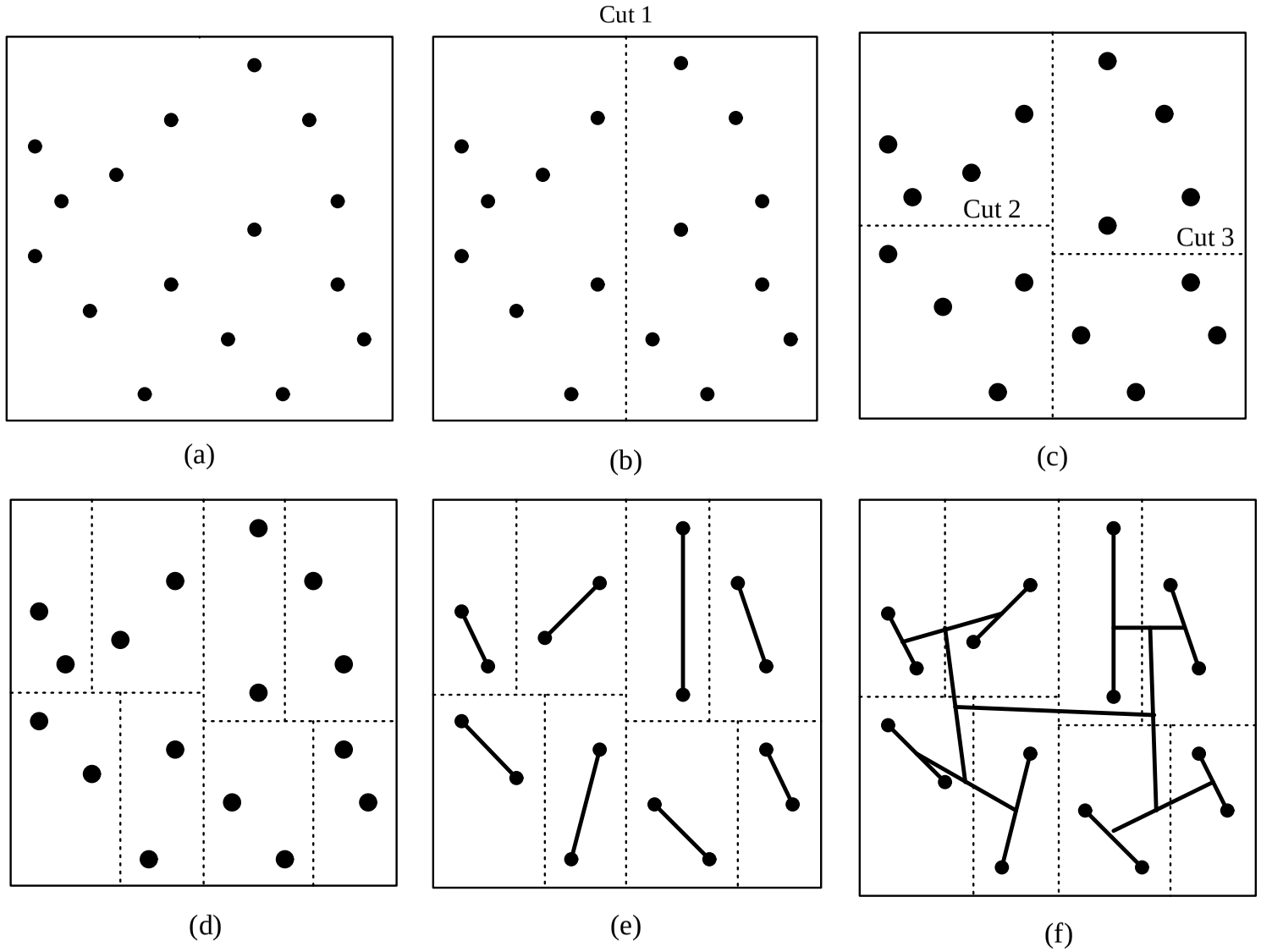
The MMM Algorithm

1. Each clock pin is represented as a point in the region, S.
2. The region is partitioned into two subregions, S_L & S_R
3. The center of mass is computed for each subregion.
4. The center of mass of the region S is connected to each of the centers of mass of subregion S_L and S_R.
5. The subregions S_L and S_R are then recursively split in Y- direction.
6. Steps 2 - 5 are repeated with alternate splitting in X- and Y- direction.

Complexity: $O(n \log n)$

~ M. A. B. Jackson, A, Sirinivasan, and E. S. Kuh, *DAC, 1990*

Routing by MMM Algorithm



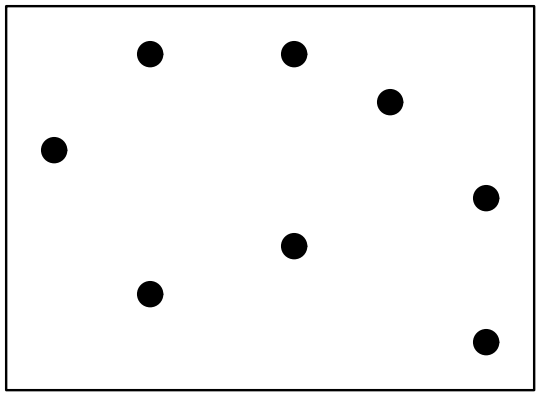
The Geometric Matching Algorithm

1. Clock pins are represented as n nodes in the clock tree ($n = 2^k$).
2. Each node is a tree itself with clock entry point being node itself.
3. The minimum cost matching on n points yields $\frac{n}{2}$ segments.
4. The clock entry point (CEP) in each subtree of two nodes is the point on the segment such that length of both sides is same.
5. Above steps are repeated for each segment.
6. If, at any stage, the edges intersect, H-filpping is applied.

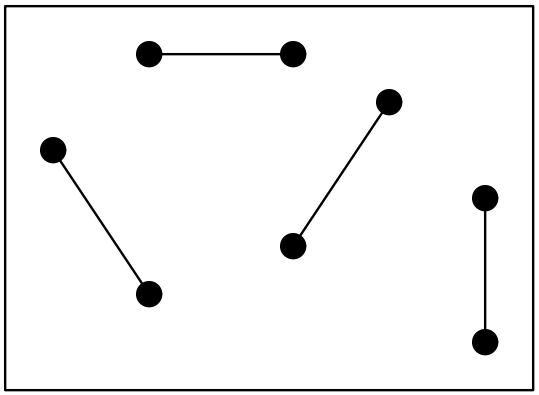
Complexity: $O(n^2 \log n)$

~ A. Kahng, J. Cong, and G. Robuns, *DAC, 1991*

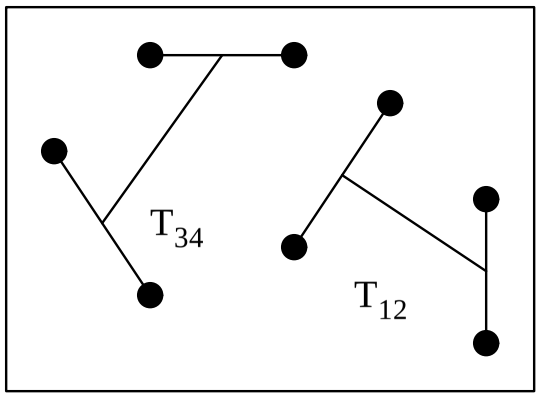
Geometric Matching Based Algorithm for 8-points



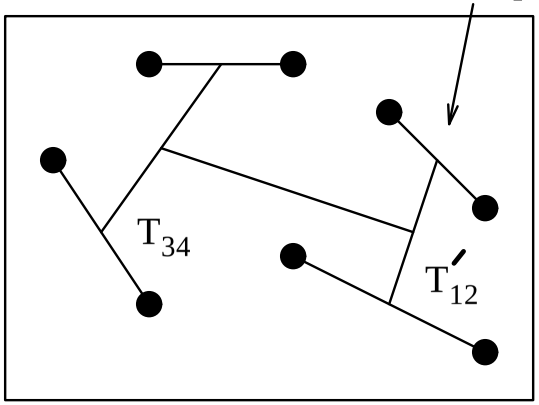
(a)



(b)



(c)



(d)

The Weighted Center Based Algorithm

1. Find the edge with the minmum weight and replace the two vertices with another vertex which lies on thier weighted center.

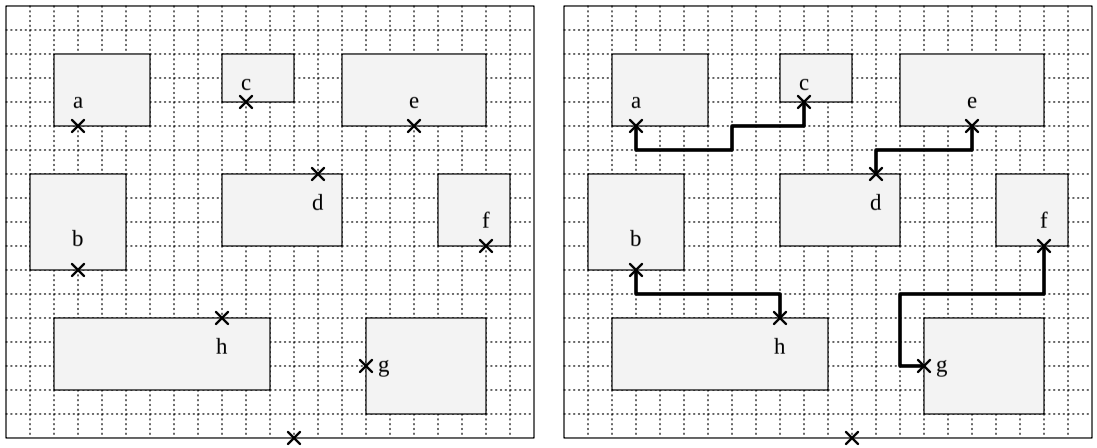
2. The weighted center is new vertex

3. The above steps are repeated recursively until all the clock terminals are joined into one global weighted center.

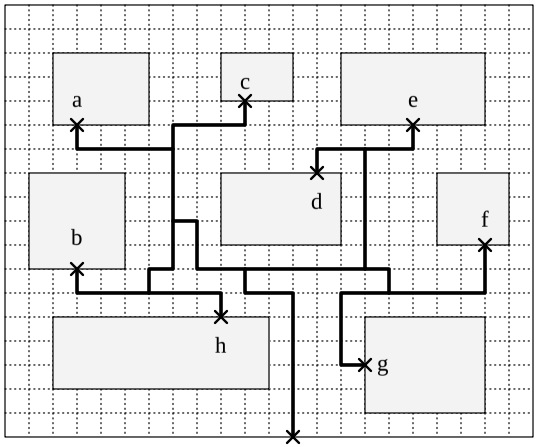
Complexity: $O(n^2)$, where n is the number of clock pins.

~ Bo and Sherwani, *ASIC Conference, 1991*

An Example by Weighted Center Algorithm



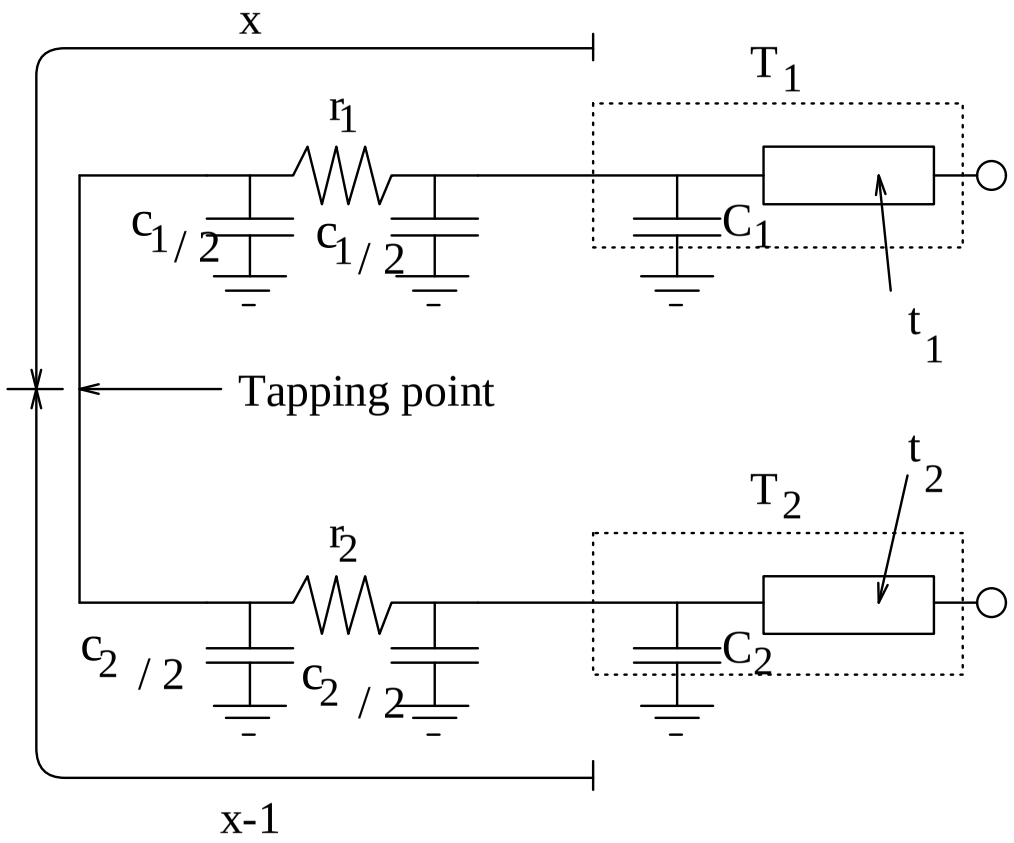
(a) (b)



(c)

Exact Zero Skew Algorithm

Merging of two trees



Tapping Point Calculation

$$x = \frac{(t_2 - t_1 + \alpha l(C_2 + \frac{\beta l}{2})}{\alpha l(\beta l + C_1 + C_2)}$$

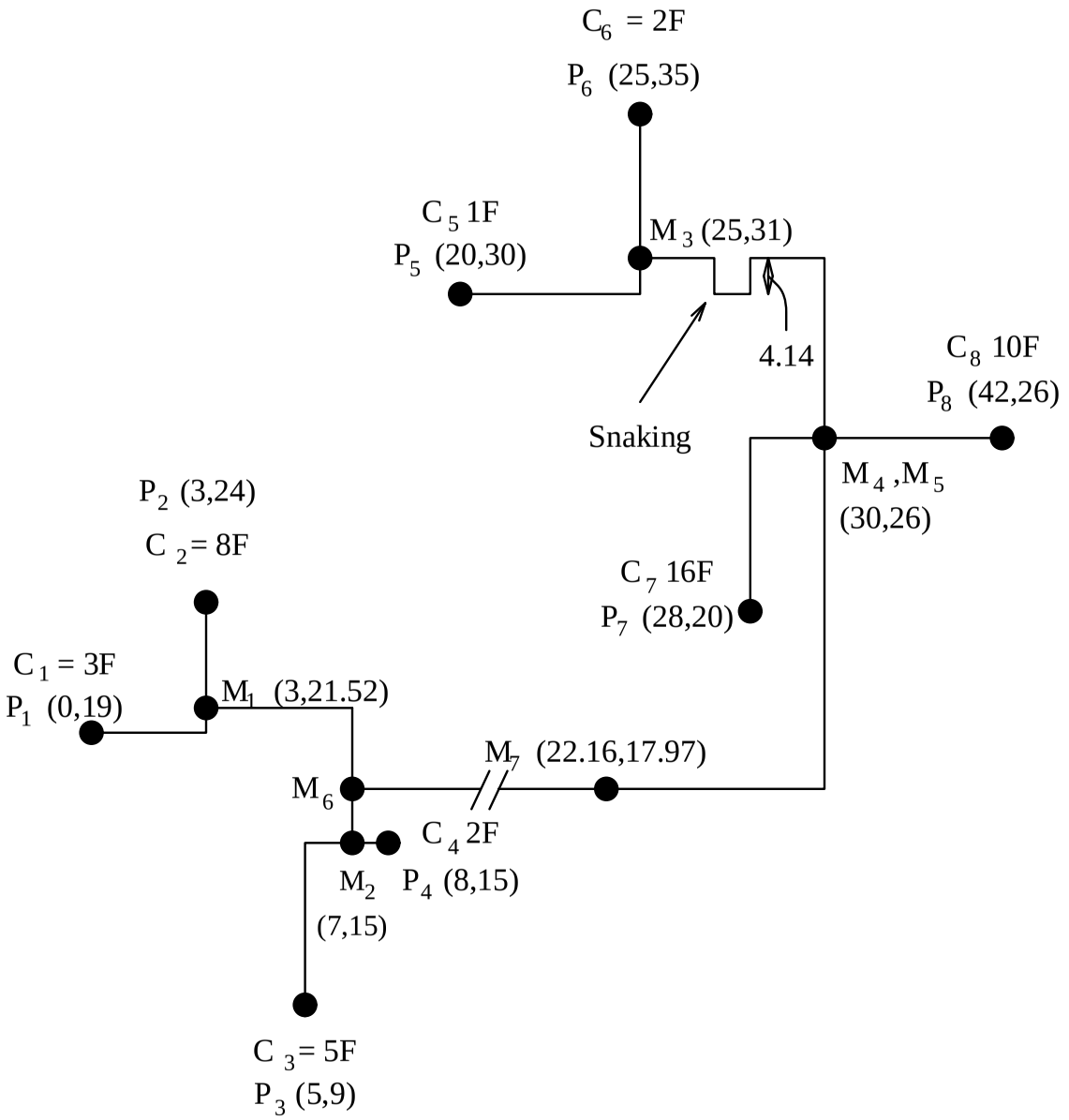
Where,

α and β are the per unit values of resistance and capacitance.

Snaking

$$l' = \frac{[\sqrt{(\alpha C - 2)^2 + 2\alpha\beta(t_1 - t_2)}] - \alpha C_2}{\alpha\beta}$$

An Example of Using Zero Skew Algorithm



Power and Ground Routing

1. In VLSI design, almost all the blocks need power supply and need to be connected to ground as well.

2. The power and ground nets are usually laid out entirely on the metal layer(s) of the chip due to smaller resistivity of metal.

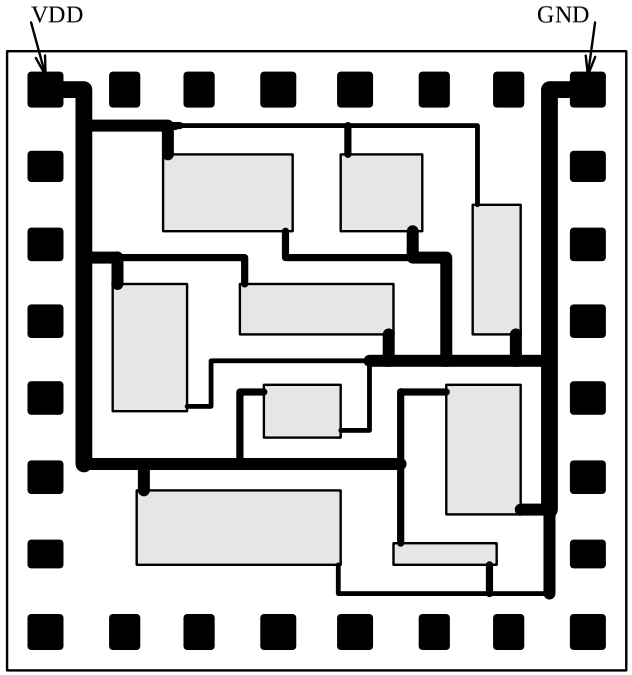
3. Since, contacts (vias) significantly add to the parasitics, it is also advisable to utilize a planar single-layer implementation of power and ground nets.

4. The widths of the segments of these nets depend on the voltage drop, current density and other constraints.

Power and Ground Routing using Interdigitated Trees

1. The power and ground nets are grown as interdigitated trees.

2. To prevent the two trees from crossing, simple traffic rules are applied to the free channels.



The width of trees at any given point must be proportional to the amount of current being drawn by the points in that subtree.