Reconfigurable ΔΣ modulator topology design through hierarchical mapping and constraint extraction

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1. Introduction

The circuits in future personal wireless communication systems must support multiple operating modes, such as AMPS, GSM, CDMA, WCDMA, and UMTS. There is few work on reconfigurable multimode ADCs [1–4]. The existing work is mostly on single-mode continuous-time ΔΣ modulators due to their power efficiency, superior linearity at low bandwidths, and inherent bandwidth resolution trade-off in the noise-shaping characteristic [5–9]. Existing automated design techniques are either customized to a few single-mode topologies [10,11] or consider ideal systems without any nonidealities [12,13]. In a recent technique proposed in [14], topologies were optimized by considering the circuit nonidealities in the modulator transfer functions (TFs). However, how the signal path coefficients are realized at circuit-level, and inherent bandwidth resolution trade-off in the noise-shaping characteristic [5–9]. Existing automated design techniques are either customized to a few single-mode topologies [10,11] or consider ideal systems without any nonidealities [12,13]. In a recent technique proposed in [14], topologies were optimized by considering the circuit nonidealities in the modulator transfer functions (TFs). However, how the signal path coefficients are realized at circuit-level was not considered during topology design. As a result, infeasible designs might occur when topologies are implemented at the circuit-level.

Next, we will use a practical design case as an example to illustrate the design difficulties that emerge as the reconfigurable modulator topology is implemented at the circuit-level. Let us consider one of the optimal topologies produced by the design methodology in [14]. The topology is shown in Fig. 1. For a required resolution and bandwidth, the method selects the modulator topology of minimum complexity and sensitivity to circuit nonidealities, including the integrator types, the oversampling ratio (OSR), and the signal path coefficients. One bit quantizers are assumed, even though the methodology supports multi-bit quantizers too. In this example, the reconfigurable modulator topologies are of orders 5, 4, and 4, respectively, for the UMTS, CDMA2000, and GSM communication modes. Parameters \( m_1, m_2, m_3 \) in the figure denote the signal path coefficients for the three operating modes UMTS, CDMA2000, and GSM, respectively.

Since the UMTS mode has the highest bandwidth requirement, a higher loop filter order was chosen to avoid using a high OSR. The channel bandwidth and dynamic range (DR) requirements for the UMTS standard are 1.92 MHz and 70 dB, respectively. The sampling frequency \( f_s \) is 150 MHz, and \( \text{OSR} = 32 \). Table 1 summarizes the modulator order and the OSR of the topology in Fig. 1.

In general, \( f_s \) must be greater than \( 2 \cdot \text{OSR} \cdot f_{in} \), such that the input signal with frequency \( f_{in} \) is oversampled by \( \text{OSR} \) times without aliasing. Thus, increasing the DR of the modulator by increasing \( \text{OSR} \) requires the circuit to operate at higher frequency, which makes the circuit-level implementation more demanding especially when the input signal bandwidth is large. The signal path coefficients are implemented as \( 1/2 \pi f_s R \)C (for active-RC...
The unity-gain bandwidth configuration was used instead of active-RC configuration. The high bandwidth requirement for the UMTS mode, the Gm-C configuration was used instead of active-RC configuration. The configuration or as $G_i/2\pi f_s C_i$ (for Gm-C configuration). Considering the high bandwidth requirement for the UMTS mode, the Gm-C configuration was used instead of active-RC configuration. The unity-gain bandwidth $(f_u)$ is determined by the transconductance $G_i$ and integrating capacitance $C_i$ as shown in the equation

$$f_u = x f_s = \frac{G_i}{2\pi C_i},$$

where $x$ is the signal path coefficient. Therefore, $f_u$ is proportional to $x$.

The following problems occur if $x$ is large:

- Eq. (1) is satisfied only if the second pole $p_2$ of the integrator is larger than $f_u$. Moreover, pole $p_2$ needs to be several times larger than $f_u$ to keep the integrator stable. A common design practice is to set the pole $p_2$ to be at least 10 times larger than $f_u$ to have 90° phase margin [15]. If coefficient $x_i$ or frequency $f_i$ are large, then the integrator needs to operate at high frequency. However, the second pole $p_2$ is limited by the parasitic capacitance and resistance of the transistors in the circuit.

- The DC gain $A_0$ can be approximated by $G_i R$. Therefore, decreasing $G_i$ will reduce $A_0$. To achieve the required DC gain, larger $G_i$ value needs to be used, which means larger $C_i$ also to keep the coefficient unchanged. However, the –3 dB bandwidth $(f_{-3dB})$ is inversely proportional to the integrating capacitance $C_i$. The DC gain can also be boosted by increasing $R$, which requires that a cascode stage could be used. However, the using of cascode configuration is limited by the supply voltage and the required signal swing.

The optimal values for parameters $G_i$ and $C_i$ need to be found considering the above circuit-level trade-offs. In addition, many other constraints may influence the topology design, such as harmonic distortion, maximum signal swing, slew rate, and so on. Neglecting the circuit-level constraints during system-level optimization might lead to infeasible designs, which increases the design cost and effort due to more iterations through the design flow being required until a constraint satisfying design is developed.

This paper presents an iterative method for designing reconfigurable continuous-time ΔΣ modulator topologies while considering circuit-level constraints. The generated topologies are optimized for their structural complexity, robustness with respect to circuit nonidealities, and feasibility at the circuit-level implementation. Circuit-level constraints are abstracted from circuit models as closed-form expressions, formulated, and then solved as a mixed-integer nonlinear programming (MINLP) problem [16]. Thus, the methodology considers the critical circuit-level constraints early in the design flow.

The methodology includes a top-down design flow, in which (i) topology mapping maps the signal path coefficients of a generic ΔΣ modulator topology to the building block parameters, followed by (ii) parameter mapping, which maps the block parameters to circuit constraints. The generic modulator topology includes the feedforward and feedback signal paths of all possible modulator topologies [14], and is used as a starting point of the design flow.

- Topology mapping analyzes alternate approaches of implementing the local feedback and feedforward coefficients of the generic topology, such as using transconductances and mirrored branches. It also considers various configurations for the building blocks of the topology, e.g., Gm-C, active RC, and OTA-OpAmp-C. A set of topology mapping rules is proposed to transform the generic topology coefficients to the circuit-level design parameters.

- Parameter mapping analyzes alternative circuit configurations that can implement the basic building blocks, such as source degenerated operational transconductance amplifiers (OTAs), OTAs with adaptive biasing, or cross coupling. The block parameters are mapped to the circuit parameters using TFs.

### Table 1: Design parameters for a reconfigurable ΔΣ modulator topology

<table>
<thead>
<tr>
<th>Order</th>
<th>OSR</th>
<th>UMTS</th>
<th>CDMA2000</th>
<th>GSM-EDGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>96</td>
<td>128</td>
<td>–</td>
<td>96</td>
</tr>
<tr>
<td>3</td>
<td>48</td>
<td>64</td>
<td>48</td>
<td>64</td>
</tr>
<tr>
<td>4</td>
<td>40</td>
<td>48</td>
<td>40</td>
<td>48</td>
</tr>
<tr>
<td>5</td>
<td>28, 32</td>
<td>40</td>
<td>40</td>
<td>48</td>
</tr>
</tbody>
</table>
2. Related work

The existing literature on reconfigurable ADC design [1–4] presents different circuit design cases, but few systematic topology design methodologies are proposed. Existing automated design methodologies are for single-mode ΔΣ modulators, only. Most of the related work is on parameter optimization for a fixed set of topologies [10,11,17,18]. Optimal parameter design for single-loop, cascaded, multibit ΔΣ modulators is discussed in [19]. The best coefficient set for each topology is generated. The impact of circuit nonidealities on system performance is not studied. Malcovati et al. [20] propose a Matlab-based behavioral simulation method for switched-capacitor (SC) ΔΣ modulators. The approach models many modulator nonidealities, such as clock jitter, operational amplifier noise, finite gain, bandwidth, slew rate, and so on. Models allow designers to perform time-domain behavioral simulations of SC ΔΣ modulators. However, no systematic design methodology is suggested to find optimal modulator architectures and design parameters.

More recently, Tang and Doboli [12] present a high-level synthesis algorithm that finds the optimal discrete-time modulator topology for a given specification. The technique solves an MINLP problem having a cost function that expresses the signal path complexity, sensitivity, and power consumption of the topology. The method considers only single-mode ΔΣ modulators built out of ideal blocks. Due to neglecting circuit nonidealities, in a real-life situation, the optimal topology generated for the ideal case might not be the best topology anymore. In [14], the reconfigurable topologies are optimized by considering circuit nonidealities through MINLP solving and post-time-domain optimization. However, there is no information on how the topologies are implemented at the circuit-level. As a result, the generated topologies may be infeasible at circuit-level design and multiple design iterations are required.

Gieling and Rutenbar [21] present an overview on techniques for automated analog system synthesis, including methods based on optimization heuristics [10,22,23], constraint satisfaction [24,25], and nonlinear [26] and geometric programming [27–29]. The top-down design flow in [24] uses constraint transformation and circuit models to select the circuit parameters that meet a system specification. The methodology does not address topology design, instead the system topology is given as an input. The top-down design method in [25] uses Genetic Algorithms and first-order circuit models to compute the circuit requirements that meet the specification of a given system topology. The top-down design flow proposed in [10] finds the coefficients of a ΔΣ modulator topology using heuristic optimization algorithms and behavioral circuit models.

In conclusion, new techniques are needed for automated synthesis of system topologies, so that the constraints due to circuit nonidealities are considered early in the design flow. Specifically, design constraints set by the circuit implementations must be incorporated into the topology selection step to improve the feasibility of the produced solutions. The work presented here attempts to address these aspects.

3. Hierarchical mapping

ΔΣ modulators can be reconfigured at three levels [14]: (1) system-level reconfiguration, which involves reconfiguring the order of the modulator, internal quantizer bits, and OSR; (2) signal-path reconfiguration, which includes modifying the signal paths and their coefficients, and (3) transistor-level reconfiguration, which means that the transconductors of the modulator are reconfigured at the transistor-level. This paper considers the first two reconfiguration levels. In addition, it allows a designer to decide which transconductors should be implemented as reconfigurable circuits. For example, if the coefficients for different modes are close (e.g., coefficients $G_{t,4}$ for the UMTS and GSM modes in Table 2), the designer may decide to realize the coefficients using transconductors that are reconfigurable at the transistor-level.

In order to generate feasible reconfigurable topologies, circuit-level nonidealities and trade-offs must be considered during topology design. However, circuit-level details are difficult to be extracted and formulated for system-level topology optimization due to the complex nature of analog circuits and their multi-dimensional performance space. In this section, a hierarchical topology mapping method is proposed, which maps the system parameters to the circuit parameters through the design hierarchy. Meanwhile, design constraints are extracted from the circuit-level to the system-level, and used for topology optimization.

The proposed methodology generates ΔΣ modulator topologies optimized for minimum design complexity, and maximum robustness with respect to circuit nonidealities. The design flow is shown in Fig. 2. First, topology mapping maps the signal path coefficients of the generic topology (in Fig. 3) to the building block parameters, such as transconductances and capacitances, by using a set of mapping rules. Then, parameter mapping maps the building block parameters to the circuit parameters through the abstract circuit models. The abstract circuit model is composed of basic functional circuit elements, like gain stages, summing amplifiers, integrators, etc. The circuit performance can be expressed as functions of the circuit parameters. Finally, circuit parameters can be further expressed as dependencies on the transistor parameters with the help of macromodels [30–34]. The third mapping step aims at giving more accurate circuit constraints, and can be formulated if circuit macromodels are available. By topology and parameter mapping, constraints and trade-offs at lower hierarchical levels are extracted to the higher

Table 2
Transconductances for the reconfigurable topology in Fig. 6

<table>
<thead>
<tr>
<th>Mode</th>
<th>$G_{t,1}$</th>
<th>$G_{t,2}$</th>
<th>$G_{t,3}$</th>
<th>$G_{t,4}$</th>
<th>$G_{t,5}$</th>
<th>$G_{t,6}$</th>
<th>$G_{t,7}$</th>
<th>$G_{t,8}$</th>
<th>$G_{t,9}$</th>
<th>$G_{t,10}$</th>
<th>$G_{t,11}$</th>
<th>$G_{t,12}$</th>
<th>$G_{t,13}$</th>
<th>$G_{t,14}$</th>
<th>$G_{t,15}$</th>
<th>$G_{t,16}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMTS</td>
<td>0.1875</td>
<td>–</td>
<td>0.5</td>
<td>1.06</td>
<td>0.2685</td>
<td>–</td>
<td>1.2</td>
<td>–</td>
<td>0.2939</td>
<td>0.1436</td>
<td>0.2684</td>
<td>0.1</td>
<td>0.1302</td>
<td>0.1</td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>CDMA2000</td>
<td>0.1081</td>
<td>0.1042</td>
<td>0.075</td>
<td>0.1631</td>
<td>–</td>
<td>0.0572</td>
<td>1.1578</td>
<td>–</td>
<td>0.0728</td>
<td>0.0134</td>
<td>–</td>
<td>0.2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>GSM</td>
<td>0.05</td>
<td>0.05</td>
<td>0.045</td>
<td>0.2865</td>
<td>–</td>
<td>0.0003</td>
<td>0.3761</td>
<td>0.2437</td>
<td>0.3045</td>
<td>0.14</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

The numbers in the table are in mS.
levels, and addressed early in the design flow. This paper focuses on the first two mapping steps, which are discussed in the next two subsections.

The design of a reconfigurable modulator is done in multiple optimization iterations. If there is no feasible solution for the selected signal path coefficients, another set of signal paths, and their corresponding coefficients are picked from the parameter sets computed by the methodology presented in [14], and post-optimized by the approach discussed in this paper. Hence, the successive optimization iterations are across the system-level, signal-path level, and circuit-level.

The effectiveness of the design flow depends on the accuracy of the extracted circuit-level constraints. The circuit-level constraints and equations can be obtained from circuit analysis [15], if one only needs a qualitative estimation of the circuit-level performance, or from behavioral models [32–35], which give more accurate predictions.

3.1. Topology mapping

The generic reconfigurable ΔΣ modulator topology proposed in [14] is shown in Fig. 3. The generic topology defines all possible signal paths of a ΔΣ modulator of any order N as each signal path can be added (removed) from the topology by closing (opening) the corresponding switch $S_i$, $U$ and $V$ are the input and output of the modulator, respectively. Blocks $I_i$ to $I_N$ are nonideal integrators. $Y_i$ is the output of the $i$th integrator, $b_i$ denotes the path from the feedback DAC to the input of the $i$th integrator, $a_i$ is the path from the input signal to the input of the $i$th integrator, and $t_{ij}$ represents the path from the output of the $i$th integrator to the input of the $j$th integrator.

Each integrator can be implemented in several ways, such as Gm-C, active-RC, and OTA-Opamp-C configurations. Each configuration has its own advantages and disadvantages. For instance, Gm-C integrators have feedforward structures, and their operating frequency range is much higher than that of the other two configurations. However, they have poor linearity and additional linearization circuits must be included. In this paper, only Gm-C integrators were considered due to the high bandwidth requirement for some of the wireless communication standards, such as UMTS and WCDMA.

**Lemma 1.** The feedforward and feedback coefficients and the integrators can be mapped to the $G_i$, $C_i$ blocks by the following rules:

$$a_i = \frac{G_{ni}}{C_i} \cdot \frac{V_{ref}}{2\pi f_s} = \frac{G_{ni}}{C_i} \cdot \frac{t_{ij}}{2\pi f_s}, \quad b_i = \frac{G_{ni}}{C_i} \cdot \frac{t_{ij}}{2\pi f_s}, \quad t_{ij} = G_{ni} \quad (2)$$

$$t_{ij} = \frac{G_{ni}}{C_j} \cdot \frac{\gamma_{ij}}{2\pi f_s}, \quad G_{ni} \quad (3)$$

where $V_{ref}$ is the gain (reference voltage) of the feedback DAC, $C_i$ is the integrating capacitance for stage $i$, and $G_{ni}$, $G_{bi}$, and $G_{ai}$ are the transconductances that implement coefficients $a_i$, $b_i$, and $t_{ij}$, respectively. For the local feedforward and feedback coefficients $t_{ij}$ and $G_{ni}$, they can be implemented as either transconductances $G_{ni}$ or mirrored branches (with gain $\gamma_{ij}$) $G_{nj}$ (Eq. (3)). Fig. 4 shows a generic configurations for stage $i$ with two alternate approaches to implement local feedforward and feedback coefficients, respectively.

**Proof.** The TF of the Gm-C integrator is $G_i/s \cdot C_i$. Let us assume that the circuit is operating at the sampling frequency $f_s$, the gain of the integrator at $f_s$ should be equal to the corresponding signal path coefficient.

Note that the proposed mapping rules and design methodology can also be extended to other configurations easily. For example,
for active-RC integrators, the equation for parameters $b_i$ in (2) is changed to $b_i = 1/(R_{bi}C_i/C_1^2\omega f s)$.

### 3.2. Parameter mapping with circuit nonidealities

The transconductance blocks $G_i$ in Fig. 4 can be implemented as highly linear operational transconductors. Several highly linear operational transconductor topologies are discussed in [36]. Based on the characteristics of the operational transconductor circuits, the parameters in the generic topology (Fig. 4) are mapped to the circuit-level parameters using the following procedure: first, parameter $G_i$ is mapped to the nonideal transconductor block, described by the nonideal TF with nonidealities, such as finite output impedance, poles, and zeros. Then, the parameters in the nonideal TF are mapped to the circuit parameters using circuit models.

While the parameters are mapped from the system-level to the circuit-level, the constraints at each design level are also extracted and formulated in the topology design. The constraints can be grouped into two categories: constraints that are critical for the modulator design, and can be formulated as closed-form expressions, so that they can be considered early in the design flow, and constraints that have secondary effects on the modulator performance, and can be handled as the circuits are designed. Next, one transconductor block with an integrating capacitor was used as an example to illustrate the parameter mapping and constraints extraction procedure.

Let us assume that the source regenerated transconductor is used. Which specific circuit configuration is utilized, like source degenerated, cross coupling, adaptive biasing, etc., is decided according to the application requirements before the parameter mapping. Fig. 5 shows the parameter mapping procedure:

1. The ideal operational transconductor amplifier (OTA) is considered (Fig. 5(a)), which corresponds to one integrating stage in the generic topology in Fig. 4.
2. A set of circuit nonidealities are included (Fig. 5(b)), and the nonideal TF is formulated as in Eq. (4). The Gm-C integrator has DC gain of $G_iR_i$, dominant pole $1/(R_iC_i)$, second pole $p_2$, and zero $z_1$:

$$\frac{V_o(s)}{V_i(s)} = \frac{G_iR_i}{1 + s/R_iC_i} \frac{1 + s/z_1}{1 + s/p_2}$$

(4)
This step determines the circuit nonidealities that are critical to the topology design. They are expressed depending on the parameters from lower design levels. Moreover, the step finds the conditions that guarantee that the neglected nonidealities have a secondary impact on the modulator performance. For example, the DC gain and dominant pole of the integrator is critical to the topology optimization, and the second pole has a secondary impact as long as it is several times larger than the unity-gain bandwidth.

3. For a specific circuit configuration, an abstract circuit model is developed, and the parameters in the nonideal TFs are mapped to circuit parameters through the abstract circuit model. For example, the abstract circuit model for source degenerated transistors is shown in Fig. 5(c). It is composed of the basic functional circuit elements for the operational transconductor, such as the source degenerated resistor, differential pair M1 and M2, biasing current, and two identical Opamps with gains $A_g$ to enhance the linearity of the circuit. The following equation is derived:

$$ V_i - A_g + \frac{1}{A_g} = V_{GS,eff} \left( 1 + \frac{b_0}{2L_0} - \frac{1 - b_0}{2L_0} \right) \tag{5} $$

By Taylor expansion, then,

$$ G_i = \frac{b_0}{V_i} = \frac{1}{R_i + \left( R_i + \frac{V_{GS,eff}}{2L_0} \right) A_g} \tag{6} $$

If $A_g \gg 1$, then $G_i \approx 1/R_i$, Eq. (6) shows the dependency of the transconductance on the circuit parameters, like the source degenerated resistance, gate override voltage $V_{GS,eff}$, and biasing current. This dependency becomes a constraint for topology design.

Fig. 5(d) is the small signal equivalent circuit for Fig. 5(c). $r_{ON}$ and $r_{OFF}$ are the equivalent impedances of the NMOS current source and PMOS active load, respectively. The circuit performance in frequency domain can be described by the parameters in Fig. 5(d). For example, the DC gain of the Gm-C integrator is expressed as $A_0 = G_{01}$ in Fig. 5(b), which equals $r_{OP}/(R_1 r_{ON})$ in Fig. 5(d), if $A_g \gg 1$. Moreover, the parameters Fig. 5(d), such as $r_{ON}$ and $r_{OFF}$, can be further expressed as functions of the transistor parameters by using circuit macromodels, and more accurate symbolic expression for the circuit parameters and performance can be obtained.

The impact of technology on the modulator performance is hard to be captured accurately and comprehensively. For example, to overcome the negative impact of technology scaling on the circuit performance (e.g., due to the lower transistor gains because of reduced supply voltages), transistors with different threshold voltages are available by using extra type of implants, masks, or thick gate oxides. Different types of transistors have very different characteristics, like transconductance, output resistance, parasitic capacitance, and so on. The designer can use different devices to make a circuit operate in its optimal operating region. Including this optimization possibility into the design flow, while requiring a large amount of characterization data, is a very interesting research topic, and will be considered in future work.

To conclude, topology and parameter mapping capture the design constraints between the design parameters at different design levels. By including these constraints in the topology optimization procedure, the generated modulator topologies satisfy the circuit-level constraints. The topology optimization procedure is presented next.

4. Design of reconfigurable modulator topology by MINLP

The state-space description of the generic topology is expressed as Eqs. (7) and (8) [14]:

$$ \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} = \begin{bmatrix} -t_{1,1} & -t_{2,1} & \cdots & -t_{N,1} \\ t_{1,2} & -t_{2,2} & \cdots & -t_{N,2} \\ \vdots & \vdots & \ddots & \vdots \\ t_{1,N} & t_{2,N} & \cdots & -t_{N,N} \end{bmatrix} \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} $$

$$ + \begin{bmatrix} b_1 - a_1 \\ b_2 - a_2 \\ \vdots \\ b_N - a_N \end{bmatrix} \begin{bmatrix} U \\ V_i \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} $$

$$ \begin{bmatrix} N_{11} \\ N_{12} \\ \vdots \\ N_{NN} \end{bmatrix} $$

$$ + E_i $$

$$ V = [f_{1,N+1} f_{2,N+1} \cdots f_{N,N+1}] + [N_{N+1} - a_{N+1}] \begin{bmatrix} U \\ V_i \end{bmatrix} $$

$$ \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} $$

where $I_i$ is the nonideal TF for the $i$th integrator, $N_{11}, \ldots, N_{NN}$ denote the circuit noise in each integrating stage, $N_{11}$ accounts for the jitter noise in the feedback DAC. Also, the nonlinearity can be modeled by calculating the TF at the harmonics of the input signal. By incorporating these nonidealities in the state-space description of the generic $\Delta \Sigma$ modulator topology, their impact on the modulator performance can be captured as closed-form expressions, and tackled early in the design flow. The derivation of the TFs of the modulator is presented in detail in [37].

For a cost function $f$, the reconfigurable topology design problem can be formulated as follows:

minimize: $$ f(x_m,i) = f(x_m,i) $$

subject to: $$ g(x_m,i) = 0 $$

subject to: $$ x_m,i \geq 0, \quad w_{x_m,i} \in [0, 1] $$

subject to: $$ x_m,i = \frac{G_m}{G_{min,i}} \frac{G_{max,i}}{f_{m,i}} $$

subject to: $$ G_{min,i} \leq G_{max,i} $$

subject to: $$ \frac{C_m}{C_{min,i}} \leq \frac{C_m}{C_{max,i}} $$

The unknowns $x_m,i$ denote the coefficients $a_i, b_i$, and $c_i$ for the $m$th mode. The unknown $w_{x_m,i}$ defines whether the signal path with coefficient $x_m,i$ is present in the topology, or not. Eq. (10) represents the $\sum_{m=1}^{M} (N_m + 1)$ equality constraints obtained from equating symbolic $L_0$ and $L_1$, to the desired loop filter functions for all $M$ modes [14]. Constraints (12) are the mapping rules, as stated in Eqs. (2) and (3). All transconductances and integrating capacitances are in the range $[G_{min}, G_{max}]$ and $[C_{min}, C_{max}]$, respectively.

The optimization variables are $x_m,i$, $w_{x_m,i}$ which are functions of $G_{max,i}$, and $G_{min,i}$, $C_{min,i}$, $C_{max,i}$, $f_{m,i}$, $R_{min,i}$, $R_{max,i}$, $R_{c,i}$, $Z_{eff,i}$, $I_{0,i}$, $V_{GS,eff,i}$, $r_{ON,i}$, $r_{OFF,i}$, $f_{OP}$, $a_N$, $a_N+1$, $f_{1,N+1}$, $f_{2,N+1}$, $\cdots$, $f_{N,N+1}$ are fixed values.

For reconfigurable $\Delta \Sigma$ modulators built with source degenerated operational transconductors, the following constraints are
also imposed:

subject to: \( \theta_{x_{ki}} = f(G_{x_{ki}}, A_{x_{ki}}, I_{x_{ki}}, V_{S,\text{eff},x_{ki}}) \) \hspace{1cm} (15)

subject to: \( A_{x_{ki}} = f(R_{\text{on},x_{ki}}, R_{\text{off},x_{ki}}, I_{x_{ki}}, A_{x_{ki}}) \) \hspace{1cm} (16)

subject to: \( R_{x_{ki}} \geq R_{\text{min}}, \quad R_{x_{ki}} \leq R_{\text{max}} \) \hspace{1cm} (17)

subject to: \( p_{1,x_{ki}} = G_{x_{ki}} R_{x_{ki}} \) \hspace{1cm} (18)

subject to: \( f_{-3 \, \text{dB},x_{ki}} = \frac{1}{2 \pi p_{1,x_{ki}}} \) \hspace{1cm} (19)

subject to: \( f_{u,x_{ki}} = \frac{A_{x_{ki}} p_{1,x_{ki}}}{2 \pi} \) \hspace{1cm} (20)

subject to: \( p_{2,x_{ki}} \geq 10 f_{u,x_{ki}} \) \hspace{1cm} (21)

subject to: \( I_{m_{ij}} = \frac{G_{x_{ki}} R_{x_{ki}}}{1 + 1/(R_{s} \eta_{m_{ij}})} \) \hspace{1cm} (22)

Constraint (15) denotes the transconductance value that can be achieved for a specific transconductor topology. This means that the transconductance for each signal path coefficients is not only limited by the range specified in Eq. (13), but also limited by the circuit parameters. The largest gain that each stage can achieve is determined by Eq. (16). Eqs. (19) and (20) are the constraints for –3 dB bandwidth, and the unity-gain bandwidth, which depends on Eqs. (16) and (18), when Eq. (21) is satisfied. Eq. (22) is the nonideal TF of the integrator used in the state-space Eqs. (7).

The used cost function is as follows:

\[
f = q_1 \sum_{m} \sum_{i,j} w_{x_{m_{ij}}} + q_2 \sum_{m_{ij}} \sum_{i,j} \left| w_{x_{m_{ij}}} - w_{x_{m_{ij}}} \right| + \sum_{m} \beta_m \sum_{k} h_{m,k}(x_{m_{ij}})
\] \hspace{1cm} (23)

The first two terms represent the topology complexity of the modulator: the first is the absolute complexity (considering the total number of signal paths in the topology) and the second term is the relative complexity (accounting for the changes of signal paths when the modulator is reconfigured). \( w_{x_{m_{ij}}} \) and \( w_{x_{m_{ij}}} \) are the binary value of the corresponding signal paths in the two modes (0 if the path is not present, and 1 if the path is present). The second term attempts to maximize the circuit sharing between modes. The third term minimizes the sensitivity of the modulator with respect to circuit nonidealties. The term is the weighted sum of the impact of \( K \) types of nonidealities on the modulator NTF, \( h_{m,k} \), a function of \( x_{m_{ij}} \), minimizes the impact of the \( k \)th nonideality on NTF for the \( m \)th mode. The considered nonidealities include finite DC gain and bandwidth of the

Fig. 6. Reconfigurable topology with transconductors and integrating capacitors.

Fig. 7. Dynamic range of the reconfigurable \( \Delta \Sigma \) topology.

Fig. 8. DR drop due to integrator finite DC gain.
integrator, circuit noise and nonlinearity. The description of functions $h_{mk}$ is presented in detail in [14].

If another integrator topology is used, only Eqs. (4)–(6) need to be re-computed. The objectives and constraints for the MINLP (Eqs. (9)–(23)) stay the same, except for the functions $f_g$ and $f_a$ in Eqs. (15) and (16), which must be modified according to Eqs. (4)–(6).

An important requirement for the proposed design flow is having accurate closed-form expressions for the relevant circuit nonidealities. Macromodeling techniques exist to formulate nonidealities in the frequency domain as TFs, Volterra series, and so on. In contrast, for time-domain (large-signal) performance, e.g., slew rate, settling time, etc., it is harder to formulate closed-form expressions using the circuit parameters as variables. Two approaches can be considered to address this issue. First, if the topology of the modulator circuits is selected before the modulator topology is optimized, closed-form expressions for time-domain constraints can be produced through curve fitting. Second, if the circuit topology is not fixed, then a generic circuit topology, such as the topology in Fig. 5(c) can be used. The generic topology incorporates only the key transistors, voltage sources, current sources, resistors and capacitors, which describe the essential characteristics of that type of circuits. Then, in addition to the topology parameters, the design flow could also compute the constraints for the detailed circuit.

The design methodology can support optimization for minimum power consumption provided that accurate closed-form expressions exist for a modulator’s power consumption. Power consumption is an important specification attribute for mobile communication systems. However, building accurate macromodels for a modulator’s power consumption is a challenging task.

5. Case study

We used the proposed design methodology to generate optimized reconfigurable ΔΣ modulator topologies that satisfy multiple specifications, have reduced system complexity, and are feasible for circuit-level implementation. We compared the
generated topologies with the topology (Fig. 1) proposed in [14]. The modulator operates in three modes that correspond to UMTS, CDMA2000, and GSM communication standards. The resolution requirements for the UMTS, CDMA2000, and GSM modes are 70, 80, and 90 dB with channel bandwidth of 1.92 MHz, 615 kHz, and 190 kHz [1].

Fig. 6 shows the optimal topology generated by the proposed design methodology. The sampling frequencies of UMTS, CDMA2000, and GSM modes are 150, 75, and 30 MHz. The corresponding OSRs of the three modes are 32, 48, and 96. The orders of the three modes are 5, 4, and 3, respectively. The UMTS mode has the highest bandwidth requirement, and thus the highest order too in order to reduce the required OSR. Switches SW2 and SW3 are closed for the CDMA2000 and GSM modes. The transconductances and capacitances for the reconfigurable topology are listed in Table 2. The integrating capacitance values are 5, 5, 40, 7.25, and 40 pF for capacitors C1 to C5. The reconfigurable topology is designed in MITLL 0.18 μm technology with 1.5 V supply voltage. Therefore, the reconfigurable modulator was scaled such that the signal swing at the output of each integrator is 0.4 V with input amplitude of 0.4 V.

Fig. 7 shows the DR of the reconfigurable topology for the three modes. The maximum SNRs that are achieved are 84, 96, and 104 dB, which are similar to the performance of the reconfigurable topology in [14]. The nonidealities of the first stage are added directly to the input signal, while the nonidealities at the following stages are attenuated by the gain of the previous stages. Therefore, the design requirement for the first stage is higher than that for other stages [2]. So, the first integrating stage is critical for evaluating the feasibility of the topology. Next, the first stage parameters for the UMTS mode were used to compare the feasibility of the topology (Fig. 6) generated by the methodology in this paper, and the topology shown in Fig. 1 from [14].

Fig. 8 shows the DR drop of the UMTS mode of the modulator in Fig. 6, when the DC gain of the first integrator equals 38 dB. The solid curve is for the ideal modulator, and the dashed curve is for the modulator with the finite DC gain of 38 dB. The smaller the DC gain is, the more the DR drops. Therefore, the DC gain needs to be larger than 38 dB in order to keep the DR drop less than 3 dB. Since C1 is equal to 5 pF, the Ga1 is 187.5 μS for the topology in Fig. 6, and 41.1 μS for the topology in Fig. 1. As a result, the DC gain of the first integrator in Fig. 1 that can be achieved is about 4.5 times smaller than that of the first integrator in Fig. 6 (Section 3.2). Hence, the design of the first integrator for the topology in Fig. 1 needs to be designed more aggressively than the integrator for the topology in Fig. 6. Fig. 9 shows the DR degradation due to the circuit noise present at the first integrator. The ideal DR of the three modes (UMTS, CDMA2000, and GSM) are plotted with dotted, dashed, and solid lines, respectively. When −60 dB white noise is added to

Fig. 13. Highly linear OTA topology.  
Fig. 14. Integrator design plan.
the first integrator, the DR of the reconfigurable modulator is degraded. The maximum achievable SNR is reduced by 3.6, 9.4, and 17.1 dB for UMTS, CDMA2000, and GSM modes, respectively.

Fig. 11 shows the DR degradation due to the nonlinearity of the first transconductor. When 2% is added to the first transconductor, the DR of the reconfigurable modulator is worsened as shown in the figure by the plots for the UMTS, CDMA2000, and GSM modes. The DR degradation is more serious for the UMTS mode, which is degraded by 15 dB. The DR degradation for CDMA2000 is 2 dB. Simulations show that a 2% nonlinearity at the first transconductor affects the performance of the GSM mode only marginally.

Fig. 12 presents the DR degradation due to the first integrator leakage. When the dominant pole of the first integrator is located at 256/\(C_2\) of the input frequency, the DR of the reconfigurable modulator is reduced as shown by the plots for the UMTS, CDMA2000, and GSM modes. The maximum achievable SNR is degraded by 7.1, 7.6, and 9 dB for UMTS, CDMA2000, and GSM modes.

Fig. 13 is the topology for the highly linear OTA used for the first integrating stage. Transistors \(M_3, M_4, M_7\) correspond to two identical amplifiers in Fig. 5(c).

Fig. 14 shows the parameter tuning plan that was used for sizing the integrator. It starts from the transconductance value \(G_m\), which is set based on the coefficient of the signal path. Then, the design is carried out by tuning the parameters to satisfy the DC gain, bandwidth, output swing, distortion, noise, and power consumption, in this sequence. If the previous performance requirement is satisfied, the design plan moves to the next requirement. Sometimes, the tuning of parameters to satisfy the next performance requirement contradicts the tuning of the previous requirement, so that the previous requirement needs to be checked again, e.g., tuning \(r_{out}\) to satisfy the bandwidth requirement, may reduce the DC gain, as shown in the figure. Theoretically, the performance parameters can be tuned in any order as long as they all meet the specification at the end. Practically, the used sequence of parameter tuning roughly follows the sequence of DC → AC → transient. Also, the main
performance trade-offs are tackled one after another, such as DC gain and bandwidth, signal swing and distortion, in order to reduce the number of iterations. Fig. 14 indicates one possible parameter tuning plan for the integrator. The dependences between the circuit parameters and the transistor sizes are detailed in the equation.

\[
\begin{align*}
I_0 & \propto \left( \frac{W}{T} \right)^{5.6} \cdot V_{BB} & \propto \left( \frac{W}{T} \right)^{7.8} \cdot V_{BP} \\
I_{out} & \propto L_{13,14} \cdot L_{1,2} \cdot \left( \frac{W}{T} \right)^{13,14} \cdot V_{cmFb} \\
A_k & \propto L_{7,8} \cdot \left( \frac{W}{T} \right)^{9,10} \cdot \left( \frac{W}{T} \right)^{11,12}
\end{align*}
\]

Equation (24)

Fig. 15 is the frequency response of the OTA. To achieve 187.5 μA transconductance for the UMTS mode, 4.07 kΩ source regenerated resistor was used. The DC gain is 46.5 dB. So, if this integrator is used for the topology in Fig. 6, the DR drop will be smaller than 3 dB. However, the DC gain drops to 27.6 dB for the same circuit with 41.1 μA transconductance. Therefore, the DR is degraded by 6.5 dB for the topology in Fig. 1, as shown in dashed-line curve with plus marker in Fig. 8. The topology generated by the proposed methodology is easier to be implemented at the circuit-level as compared to the topology in [14] because of considering the extra circuit-level constraints during the topology design.

Fig. 16 shows the complete layout of the OTA circuit. The transistor pairs that need to be matched are drawn in a common-centroid way. The two integrating capacitors are arranged in a 4 × 5 array, each of which equals 0.498 pF. The OTA is laid on the bottom-right corner of the chip, which is very close to the input/output pads, so the voltage drop along the metal wire is negligible. Figs. 17 and 18 are the post-layout simulation results in frequency-domain and time-domain, which are similar to the simulation results at the circuit-level. The differential output voltage swing is 401.5 mV. The total power consumption for the OTA is 886 μW.

6. Conclusion

This paper proposes a methodology for designing reconfigurable continuous-time ΔΣ modulator topologies while considering constraints that express the circuit-level implementation requirements. By hierarchically mapping the generic topology parameters to the circuit parameters, circuit-level constraints are abstracted and formulated in the topology optimization program. Topologies are optimized for minimizing the complexity of the topologies, maximizing the topology robustness with respect to circuit nonidealities, and maximizing the feasibility at circuit-level implementation. The presented case study for designing topologies for a three mode reconfigurable ΔΣ modulator shows that the topology generated from the proposed methodology avoids the design difficulties as compared to the topology in [14], such as the high DC gain requirements with large transconductance of the integrators.

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