Reconfigurable Switched-Capacitor ΔΣ Modulator Topology Design

Ying Wei, Pengbo Sun, Alex Doboli
Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY, 11794-2350

Abstract—In this paper, a methodology for designing reconfigurable discrete-time ΔΣ modulator topologies is proposed. Topologies are generated from a set of all possible topologies expressed by a generic topology, and optimized for minimizing the complexity of the topologies, maximizing the topology robustness with respect to circuit nonidealities, and minimizing total power consumption. The paper presents a case study for designing topologies for a three-mode reconfigurable ΔΣ modulator. The paper also offers a reconfigurable topology implementation on a Programmable System-on-Chip (PSoC) device.

I. INTRODUCTION

The rapid development in wireless technologies has led to a demand for reconfigurable receiver-on-a-chip that supports multiple standards. In the multi-standard receiver implementation, the major difficulty falls in the design of high performance, compact multimode analog to digital converters (ADC), because of the different requirements (e.g. dynamic range (DR) and bandwidth) between different modes [1].

There is little understanding on how to develop optimal reconfigurable topologies for a new set of modes. Also, to improve design closure and reduce cost, topology design must contemplate a fair amount of circuit nonidealities. More efficient methodologies are needed for systematically designing reconfigurable ADCs while contemplating nonidealities early in the design flow.

Current design methodologies are for single-mode ΔΣ only. Most of the work is on topology parameter optimization with limited modification of the modulator topology. Medeiro et al. [4] propose a design flow based on extensive analysis and modeling of the nonidealities that degrade the ΔΣ modulator performance. However, their methodology is limited to the four single-mode, discrete-time topologies supported by CAD tools – SDOPT and FRIDGE. Francken et al. [5] describe an approach for high-level simulation and synthesis of discrete-time ΔΣ modulators. Behavioral models for integrators, quantizer, and feedback digital-to-analog converter (DAC), are integrated in a synthesis tool (DAISY) that selects the modulator topology with the lowest power consumption for a given specification and constraints for the building blocks. An analytical integration method for the simulation of continuous-time ΔΣ modulators is suggested in [7]. However, the set of allowed topologies is not complete, thus optimal solutions might be missed. Tang and Doboli [6] present a synthesis algorithm that finds the optimal topology for a given specification by solving a mixed-integer nonlinear programming (MINLP) problem [10] with a cost function expressing the signal path complexity, sensitivity, and power consumption of the topology. This method considers only single-mode ΔΣ modulators built out of ideal blocks.

This paper proposes a systematic methodology for designing reconfigurable discrete-time ΔΣ modulator topologies, optimized for minimum topology complexity, maximum robustness to circuit nonidealities, and minimum power consumption. The methodology is based on the concept of generic topology that expresses all possible signal paths in a reconfigurable topology. We present the modeling of generic topologies including following nonidealities: integrator leakage and gain error, circuit noise, and nonlinearity. Models are used in the methodology to set up a set of nonlinear equation sets. Equations are solved for finding efficient reconfigurable topologies. Found topologies are then refined using Simulink simulation of models with more detailed nonidealities. The design methodology is presented in Section II. The paper presents a case study for designing topologies for a three-mode reconfigurable ΔΣ modulator, and the implementation of a second-order reconfigurable topology on PSoC, as discussed in Section III.

II. OVERVIEW OF THE METHODOLOGY FOR RECONFIGURABLE ΔΣ MODULATOR TOPOLOGY DESIGN

In this section, we will use a dual-mode third-order reconfigurable ΔΣ modulator as example to show the design methodology, which can be generalized to reconfigurable ΔΣ modulator of any order.

The input to the topology design methodology is the specifications for the dual-mode reconfigurable ΔΣ modulator. For each target specifications, such as DR, a set of solutions that can achieve the target DR are found by using analytical expressions, such as the expressions embedded in the ΔΣ toolbox [9]. Each solution has four parameters: (i) the order of the loop filter, (ii) the oversampling ratio (OSR), (iii) the internal quantizer bits, and (iv) the noise transfer function (NTF) type, Butterworth or Inverse Chebyshev. Any solution for a single mode can be combined with the solution for another mode to build a dual-mode ADC. Hence, the set of possible candidates for the dual-mode reconfigurable ADC are generated. Each candidate can be implemented using different topologies, and optimal topologies are generated by the proposed methodology.

Optimal reconfigurable ΔΣ modulator topologies are designed for a set of specifications starting from a generic modulator topology. The generic topology contains all possible signal paths in a reconfigurable modulator. The generic topology for a third order modulator is shown in Fig. 1.

The state-space description of the topology is expressed as follows:
the signal path with coefficient $x_g$ derived from the state-space equations.

By equating symbolic expressions for $L_1$ variables integrator, the integrator leakage and gain error are modeled $N_{vh1}$, $N_{vh2}$, and $N_{vh3}$ denotes the circuit noise in each integrating stage.

By solving the state-space equations, the transfer function of the modulator is written as equation $V = L_0 U + L_1 V + E_q$ [8]. Variables $L_0$ and $L_1$ are loop filters, which can be analytically derived from the state-space equations.

**MINLP formulation.** For a cost function $f$ (expressing the desired design goals), the problem of designing an optimized reconfigurable topology is formulated as

$$\text{minimize } f = f(x_{m,i}, w_{x_{m,i}});$$

subject to: $g(x_{m,i}) = 0$;

subject to: $x_{m,i} \geq 0$, $w_{x_{m,i}} \in \{0, 1\}$;

Variable $x_{m,i}$ denotes any of the unknown coefficients $a_i$, $b_i$, and $t_i$ for the $m$th mode. Unknown $w_{x_{m,i}}$ represents whether the signal path with coefficient $x_{m,i}$ is present in the optimal topology or not. $g$ are the 24 equality constrains obtained from equating symbolic expressions for $L_0$ and $L_1$ to the desired loop filter functions for all the modes [6].

The cost function for optimal reconfigurable modulator topology design is

$$f = \alpha_1 \sum_i x_{m,i} + \alpha_2 \sum_{i,j} \sum_{m=1}^{3} |x_{m,i} - w_{x_{m,i}}| + \sum_i \beta_i \left( \sum_{m} h_{mk}(x_{m,i}) \right) + \gamma \sum_{m} \sum_{i} \rho_{m,i} $$

(2)

The first two terms in the cost function represent the complexity of the modulator topology. The first term is the absolute complexity, considering the total number of signal paths in the topology. The second term is the relative complexity that accounts for the changes of the signal paths when the modulator is reconfigured.

The third cost function term minimizes the sensitivity of the modulator with respect to circuit nonidealities. The term is the weighted sum of the impact of nonidealities on the modulator NTF. $h_{mk}$, a function of $x_{m,i}$, minimizes the impact of the $k^{th}$ nonideality on NTF for the $m$th mode, which captures the following nonidealities. 

**Integrator leakage and gain error:** for switched-capacitor integrator, the integrator leakage and gain error are modeled by including the finite gain ($A_i$) of the OpAmp and capacitor mismatch factor ($e_i$) in the integrator transfer function $I_i$, respectively, as shown below.

$$L_i = g_i (1 - e_i) \frac{(1, z)_{i}}{z - (1 - g_i/A_i)}, \quad i = 1, 2, 3$$

Where, $g_i$ is the integrator gain, $(1, z)$ denotes two types of integrators: delayed or delayless. Notice that the NTF only depends on the loop filter $L_1$. Therefore, minimizing the variation of the NTF is equivalent to minimizing $L_1$. If the integrator transfer function is replaced by equation (3), then $L_1$ becomes to equation (4).

$$L_1 = L_{1, \text{num}} + \frac{\sum_{i=1}^{3} \beta_i \left( \sum_{j=0}^{2} \rho_{ij} \cdot z^j \right)}{L_{1, \text{den}} + \sum_{i=1}^{3} \beta_i \left( \sum_{j=0}^{2} \rho_{ij} \cdot z^j \right)} + \sum_{i=1}^{3} \epsilon_i \left( \sum_{j=0}^{2} \theta_{ij} \cdot z^j \right) $$

(4)

Variable $L_{1, \text{num}}$ and $L_{1, \text{den}}$ denotes the denominator and numerator of the ideal loop filter function $L_1$, respectively. $\rho_{ij}$, $\theta_{ij}$, $\epsilon_{ij}$, $\delta_{ij}$ are the symbolic coefficients as functions of signal path coefficients. To minimize the difference between $L_1$ and $L_1$, the following function $h_{mk}$ was added to the overall cost function (2) used in topology design:

$$h_{mk} = \sum_{i=1}^{N} \sum_{j=0}^{3} \left( |\epsilon_{ij}| + |\delta_{ij}| + |\epsilon_{ij}| + |\delta_{ij}| \right)$$

(5)

**Circuit noise and nonlinearity:** Considering the noise of all integrating stages, the transfer function of the modulator was expressed as equation (6). And, equation (7) captures the circuit noise in the cost function.

$$V = L_0 U + L_1 \bar{V} + \frac{\sum_{i=1}^{3} \sum_{j=0}^{3} \epsilon_{ij} \cdot z^j}{L_{1, \text{den}}} \cdot N_{vh,i} + E_q $$

(6)

$$h_{mk} = \sum_{i=1}^{N} \sum_{j=0}^{3} \left( |\delta_{ij}| + |\delta_{ij}| \right) $$

(7)

In the frequency domain, nonlinearity can be modeled by calculating the frequency responses at different harmonic. For example, let assume that only the second order nonlinear component ($k_2$) of the first stage is considered. Then, the frequency response of the modulator can be expressed as

$$L_1 \approx L_{1, \text{num}} + k_2 \frac{\sum_{j=0}^{3} \delta_{ij} \cdot z^j}{L_{1, \text{den}} + k_2 \sum_{j=0}^{3} \delta_{ij} \cdot z^j} $$

(8)

The corresponding term in the cost function (2) is

$$h_{mk} = \sum_{i=1}^{N} \left( |\delta_{ij}| + |\delta_{ij}| \right) $$

(9)

The forth cost function term minimizes the power consumption. It takes into account the static and dynamic power consumption of the switched-capacitor loop filter, which has the same form as that in [6].

By formulating the reconfigurable modulator topology synthesis problem as a MINLP problem, and including the above-mentioned four nonidealities into the cost function, a set of topologies is generated.

**III. CASE STUDIES**

**A. Triple-mode reconfigurable ΔΣ modulator topology design**

We used the proposed design methodology to generate optimized reconfigurable ΔΣ modulator topologies that satisfy multiple specifications, and have reduced system complexity. The modulator operates in three modes that correspond to UMTS, CDMA2000, and GSM communication standards. The DR requirement for UMTS, CDMA2000, and GSM are 11.5-bit, 13-bit, and 15-bit with the bandwidth of 1.92MHz, 615kHz, and 190kHz, respectively [1].
One of the optimized topologies is shown in Fig. 2. Table 1 presents the comparison of the two optimized topologies obtained using the proposed methodology, and a non-reconfigurable topology that includes three single-mode modulators. The comparison is in terms of the topology complexity, reduction in design effort (η_d), and power consumption (η_p). Topology opt1 has orders < 4, 4, 4 > for the three modes. Topologies opt2 has orders < 4, 3, 3 > for the three modes. The complexity of the system is analyzed with respect to the number of signal paths (N_p), the number of non-reconfigurable cells (N_c,r), and the number of reconfigurable cells (N_c,r).

Table I shows that reconfigurable ADCs are much more compact than the modulator built out of three single-mode architectures. For example, there are 33 signal paths in the non-reconfigurable topology, while there are only 25, 20 signal paths in the generated topologies opt1, opt2, respectively. Less number of signal paths not only decreases the complexity of the circuit implementation, but also decreases the overall power consumption and chip area. Design effort is estimated from the number of signal paths and the number of reconfigurable cells.

In order to analyze the robustness of the produced modulator topologies, we simulated the second mode of topologies opt2. Fig. 3 presents the performance comparison for mode 2 of topology opt2 and the corresponding ΔΣ toolbox topology in the presence of circuit noise and integrator leakage. The generated topology performs better. If circuit noise is considered (Fig. 3(a)), the improvements of peak SNR for mode 2 of topology opt2 is 3dB and 10dB as compared to the toolbox topology for noise levels of −70dB and −60dB, respectively. The higher the noise level, the more the improvement. Fig. 3(b) shows the SNR comparison for integrator leakage. For example, if the OpAmp of the first integrator has finite gain of 50dB or 60dB, the degradation of SNR because of integrator leakage for mode 2 of topology opt2 is 3dB less than that of the toolbox topology, as shown by the dashed line and the dashed-dotted line with plus markers, respectively. Therefore, although in the ideal case the generated topologies behave the same as the topologies from the ΔΣ toolbox, the optimized topologies are more robust in the presence of circuit noise. The performance improvement shows that the third cost function term is crucial to the performance of the final reconfigurable topologies, as it captures the possible performance tradeoffs for the topologies with respect to circuit nonidealities.

### Table I

<table>
<thead>
<tr>
<th>Topology</th>
<th>N_p</th>
<th>N_c,r</th>
<th>N_c,r</th>
<th>η_d</th>
<th>η_p</th>
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<td>non-reconfigurable</td>
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<td></td>
<td></td>
<td></td>
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<td>opt1 &lt; 4, 4, 4 &gt;</td>
<td>25</td>
<td>18</td>
<td>7</td>
<td>30.2%</td>
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<tr>
<td>opt2 &lt; 4, 3, 3 &gt;</td>
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<td>15</td>
<td>5</td>
<td>39.4%</td>
<td>24.2%</td>
</tr>
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</table>

**Fig. 2.** Reconfigurable modulator topology opt2

**Fig. 3.** SNR degradation by circuit nonidealities for topology opt2 (mode 2)

**Fig. 4.** PSoC analog system [11]

### B. Implementation of reconfigurable ΔΣ modulator on PSoC

The PSoC family consists of many mixed-signal arrays with on-chip controller devices. The top level analog architecture is shown in Fig. 4. Analog PSoC block array consists of four analog columns, each of which consists of three analog blocks: one continuous-time (CT) block and two switched-capacitor (SC) blocks. The analog SC blocks support ΔΣ, successive approximation, and incremental ADC conversion, capacitor DACs, and SC filters. They have three input arrays (ACAP, BCAP, and CCAP) and one feedback array (FCAP) of binary-weighted switched-capacitors, allowing user programmability of the capacitor weights. This provides summing capability of two scaled inputs and a non-switched capacitor input. ACAP, BCAP, and CCAP range from 1C to 32C, and FCAP has value of 16C or 32C, where C is the unit capacitance of the capacitor array [11].

A second-order ΔΣ modulator can be implemented by using two SC blocks as the integrators. We designed a dual-mode second-order topology. The target peak SNR for the two modes are 10 bits (60dB) and 8 bits (48dB), respectively. The two modes have five and six signal paths with OSR of 64 and 40, respectively. NTF types for the two modes are Butterworth type, and Inverse Chebyshev type, respectively. When the
modulator is switched from one mode to another mode, four signal paths need to be reconfigured: signal path coefficients \(a_1, a_2, b_1\) need to be modified, and one more signal path \(t_{2,1}\) needs to be switched on for the second mode, as shown in Fig. 5(a).

The implementation of the topology on PSoC is shown in Fig. 5(b). The coefficients \((a_1, a_2, b_1)\) of the signal path can be modified by changing the capacitor arrays (ACAP and FCAP). The additional signal path \(t_{2,1}\), when the modulator is reconfigured, is implemented by using one more input array (BCAP) for the first SC block. The values of the capacitor arrays are shown in Table II.

Fig. 6 shows the simulation results. It shows that the peak SNR of the two modes equals to \(71dB\) and \(60dB\) for the ideal modulator, respectively. If circuit nonidealities are considered, the peak SNR drops to \(60dB\) and \(54dB\), respectively, which can still meet the design specifications. Fig. 7 shows the output spectrum from the measurement. The input is 2.1V peak-to-peak sinusoidal wave with frequency of 45kHz. For mode 1, the noise floor level is about \(-55dB\), and the SNR is about \(60dB\).

**TABLE II**

<table>
<thead>
<tr>
<th>Mode</th>
<th>SC block 1</th>
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<th>SC block 2</th>
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<tr>
<td></td>
<td>ACAP</td>
<td>BCAP</td>
<td>FCAP</td>
<td>ACAP</td>
</tr>
<tr>
<td>1</td>
<td>4C</td>
<td>–</td>
<td>16C</td>
<td>8C</td>
</tr>
<tr>
<td>2</td>
<td>8C</td>
<td>1C</td>
<td>32C</td>
<td>16C</td>
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**REFERENCES**