

Digital Cell Macro-model with Regular Substrate Template and EKV Based MOSFET Model

ABSTRACT

This paper presents substrate noise macro-models for standard digital cells like INV, NAND and BUFFER. The macro-models are based on a scalable substrate network template and a simple structural MOSFET model equivalent to EKV model. Symbolic expressions are derived for the substrate voltage, injection current and output voltage of each primary digital cells. Proposed models contain physical detail of the device and process, therefore they are valid for different processing technology and input transition, and are more accurate as compared to the macro-model generated from Spice simulation and curve fitting. Our macro-models are accurate within 5-10% from SPICE simulation with the full circuit and MOSFET model, and the simulations are at least 4 times faster. With this model we can predict spatially and temporally the occurrence of substrate noise peaks in a digital design.

1. INTRODUCTION

Serious noise coupling problems are emerging in mixed-signal systems-on chip, because of the noisy nature of the digital circuits and the low noise tolerance of analog circuits [6]. The switching noise generated by digital blocks propagates through the substrate to the sensitive parts of the SOC, e.g., RF and analog circuits, dynamic logic and memory circuits. The supply and substrate connection networks also contribute to noise generation through inductances of bond wires. Many orthogonal factors, such as layout geometry and process technology contributes to the substrate noise characteristics of a design. The *temporal* (time behavior) and *spacial* (position of noise sources) dependencies are both important factors in noise modeling of SOC.

Substrate modeling techniques based on device simulator [3], Finite Differential Methods (FDM that solves Poisson equations), and Boundary Element Methods (BEM that solve Green's functions) [8, 9] generally achieves high accuracy. However, they require tedious computation and large memory spaces, which are unsuitable for circuit and system synthesis. As an alternative, it is beneficial to generate substrate macro-models [1, 6] for digital cells using RC elements to describe the substrate behavior.

Many substrate macro-models use equivalent current sources, called noise signature [1], to model the noise injection [4, 5,

2]. The noise signature is generated from SPICE simulation of the digital cell and stored as a look-up table[1]. The main disadvantage of these methods is the requirement of current source tuning to get the accurate model for different transition time and device technology. However, there is no suggestion for a general algorithm to control the tuning process, and also there is not much insight provided into the device physics through adjustment of the equivalent noise sources.

In order to solve the problem, we propose noise macro-models that physically describe power/ground coupling, substrate coupling, and MOSFET coupling. The substrate network model is based on the BEM substrate extraction, but in a compact and regular topology so that it can be easily applied to all the digital cell in the standard library. The MOSFET macro-model is derived symbolically from EKV model [10]. The model maintains the physical information on the digital cell and is valid over different processing technology and input transitions. The speed of the symbolic simulation is at least 4 times higher than SPICE simulation. The accuracy of our model is much higher compared with digital cell macro-model without MOSFET, and is within 5-10% from SPICE simulation with full digital cell model (including MOSFET). For comprehensive cells, the macro-model can be composed of primary cells' macro-model.

The paper has the following structure. Section 2 discusses the modeling and noise simulation flow. Section 3 presents the substrate and MOSFET macro-model. Section 4 introduces digital cell macro-model example digital cell macro-model such as inverter, nand2, and buffer. Section 5 discusses simulation results. Finally, conclusions are provided.

2. MODELING AND SIMULATION FLOW

A large digital design is generally composed of digital library cells. To analysis the switching noise characteristics of a digital design, it is beneficial to setup noise macro-models for library cells and use the composition to get noise model of the whole design. Accurate composition is difficult to achieve, because both the temporal and spacial dependencies of noise injection at different point of the layout needs to be understood. In our modeling methods, the substrate network template provides noise spacial dependency information. The temporal noise dependency information is provided by the transient analysis of the primary cells and the composed cells.

The modeling and design flow is shown in Figure 1. We used standard library cells TSMC025 μ m and TSMC035 μ m digital cell libraries [13]. The substrate macro-model is generated based on the BEM layout extraction in SPACE[7]. It has a regular topology because of the same layout style and contact pattern in the digital cell. The MOSFET macro-model is derived from EKV transistor model. The digital-cell macro-model is obtained through symbolic derivation of the electrical property of the MOSFET connection, substrate network, and power/ground parasitics.

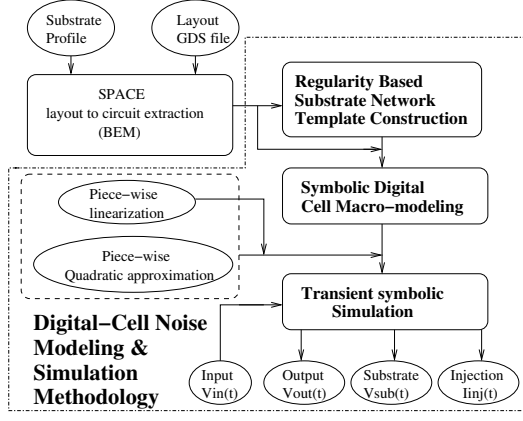


Figure 1: Digital cell substrate network extraction and noise simulation flow

We propose to implement symbolic simulation [11] instead of SPICE numerical simulation in order to reduce the simulation time, memory storage and avoid convergency problems by optimizing the symbolic expressions. It also provides insight into the noise dependencies and simulation error control, which is helpful for noise modeling and noise model composition for larger circuits.

3. SUBSTRATE AND MOSFET MODELS

Generally the substrate parasitic of random circuit design is difficult to predict. However, for digital library cells, the same layout style can be observed, which leads to a fixed substrate contact pattern and regular parasitic network topology. As an example, Figure 2 shows the regular substrate parasitic extracted from Nand2 in TSMC025 digital cell library. This section presents general substrate network template and extraction steps. More detailed information are offered in [14].

3.1 Substrate network template

The substrate template was shown in Figure 3. c_n is the capacitance between the transistor body to the substrate node, r_n is the resistance between the transistor body to the substrate node, $r_{n,0}$ is the resistance between the transistor body and the ground line substrate contact. $r_{n,n-1}$ is the resistance between two transistor body nodes. We characterized the electrical behavior of this template, and derived the following symbolic model:

A. Substrate model for pull-down network (p substrate, n diffusion):

$$I_{injn}^T = Gm_n V_{injn}^T \quad (1)$$

Where I_{injn} , V_{injn} are the substrate injection current and voltage arrays. Gm_n is the general admittance matrix for

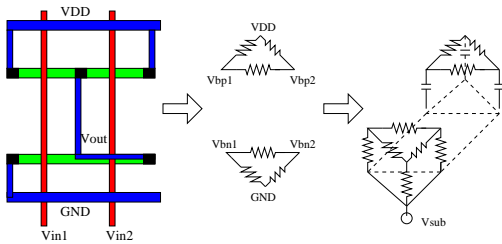


Figure 2: Nand2 substrate network mapped to layout style

substrate.

$$I_{injn} = [I_{injn_0} \ I_{injn_1} \ \dots \ I_{injn_{n-1}} \ I_{injn_n}] \quad (2)$$

$$V_{injn} = [v_{bn_n} \ v_{bn_{n-1}} \ \dots \ v_{bn_0} \ v_{bn_{sub}}] \quad (3)$$

$Gm_n =$

$$\begin{bmatrix} \frac{-1}{r_{n,0}} & \frac{-1}{r_{n-1,0}} & \dots & \frac{-1}{r_{1,0}} & (\sum_{i=1}^n \frac{1}{r_{i,0}} + \frac{1}{r_0}) & \frac{-1}{r_0} \\ 0 & \dots & \frac{-1}{r_{2,1}} & (\frac{1}{r_{2,1}} + \frac{1}{r_{1,0}} + \frac{1}{r_1}) & \dots & \frac{-1}{-r_1} \\ \dots & \dots & \dots & \dots & \dots & \dots \\ (\frac{1}{r_{n,n-1}} + \frac{1}{r_{n,0}} + \frac{1}{r_n}) & \frac{-1}{r_{n,n-1}} & \frac{-1}{r_{n,n-2}} & \dots & \frac{-1}{r_{n,0}} & \frac{-1}{r_n} \end{bmatrix} \quad (4)$$

B. Substrate model for pull-up network (p substrate, n well and p diffusion):

$$I_{inj p}^T = Gm_p V_{inj p}^T + Gm_{p0} V_{inj p0}^T \quad (5)$$

Where $I_{inj p}$, $V_{inj p}$ are the substrate injection current and voltage arrays. Gm_p , Gm_{p0} are state variable admittance matrix for parasitics.

$$I_{inj p} = [I_{inj p_0} \ I_{inj p_1} \ \dots \ I_{inj p_{n-1}} \ I_{inj p_n}] \quad (6)$$

$$V_{inj p} = [v_{bp_n} \ v_{bp_{n-1}} \ \dots \ v_{bp_0} \ v_{bp_{sub}}] \quad (7)$$

$$V_{inj p0} = [v_{bp0_n} \ v_{bp0_{n-1}} \ \dots \ v_{bp0_0} \ v_{bp0_{sub}}] \quad (8)$$

$Gm_p =$

$$\begin{bmatrix} \frac{-1}{r'_{n,0}} & \dots & \dots & \frac{-1}{r'_{1,0}} & (\sum_{i=1}^n \frac{1}{r'_{i,0}} + \frac{C_0}{h}) & \frac{-C_0}{h} \\ 0 & \dots & \frac{-1}{r'_{2,1}} & (\frac{1}{r'_{2,0}} + \frac{1}{r'_{1,0}} + \frac{C_1}{h}) & \dots & \frac{-C_1}{h} \\ \dots & \dots & \dots & \dots & \dots & \dots \\ (\frac{1}{r'_{n,n-1}} + \frac{1}{r'_{n,0}} + \frac{C_n}{h}) & \frac{-1}{r'_{n,n-1}} & \dots & \dots & \frac{-1}{r'_{n,0}} & \frac{-C_n}{h} \end{bmatrix} \quad (9)$$

and $[Gm_{p0}] =$

$$\begin{bmatrix} 0 & \dots & \dots & \frac{-C_0}{h} & \frac{C_0}{h} \\ \dots & \dots & \dots & \dots & \dots \\ 0 & \frac{-C_{n-1}}{h} & \dots & \dots & \frac{C_{n-1}}{h} \\ \frac{-C_n}{h} & 0 & \dots & 0 & \frac{C_n}{h} \end{bmatrix} \quad (10)$$

C. Extraction steps:

Based on the SPACE extraction results, we concluded the following procedures for extracting substrate parasitics of a standard digital cell:

Step1: Set VDD/VSS line as $node_0$ in the substrate network.

Step2: Number the NMOS/PMOS transistor from left to right as 1 to n .

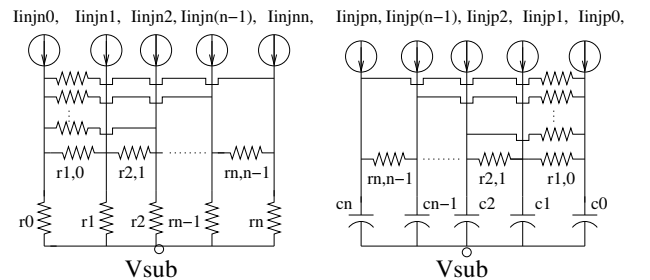


Figure 3: Substrate noise injection network template

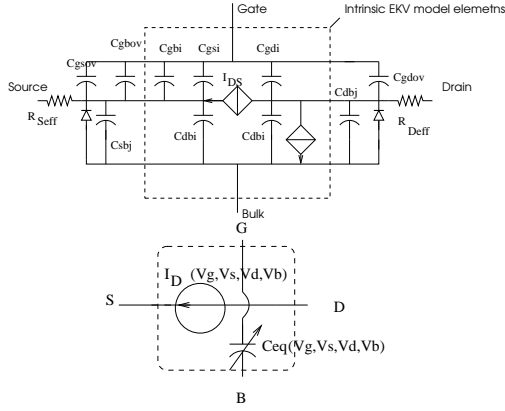


Figure 4: MOSFET macro-model derived from EKV transistor model[11]

Step3: Introduce a parasitic resistance $r_{n-1,n}$ between transistor $NMOS_{n-1}, NMOS_n$ or $PMOS_{n-1}, PMOS_n$.

Step4: Introduce a parasitic resistance $r_{n,0}$ between $NMOS_n / PMOS_n$ and VSS/VDD.

Step5: Introduce a parasitic resistance r_n between transistor $NMOS_n / PMOS_n$ and substrate node V_{sub} .

3.2 MOSFET macro-model

The MOSFET macro-model is derived based on the EKV model [10], as shown in Figure 4, and included in the derivation of the noise injection model for each digital cell. As compared to SPICE 1-3, and BSIM 1-3 [12], this model symmetrically treats the source and drain with the substrate node as the voltage reference point, and offers inversion charge model closer to device physics. The model uses compact form to treat weak inversion-strong inversion transition and the linear region-saturation region transition at the same time.

In order to generate compact digital cell noise macro-model, we derived a simplified structure to represent the EKV transistor model, which decouples the current flow of the MOSFET channel with the injection current into the body node based on MOSFET charge conservation. Figure 4 shows the EKV transistor model and our macro-model. The macro-model preserves the same electrical characteristics by using comprehensive expression for the equivalent capacitor.

The MOSFET current model I_D is expressed as:

$$I_D = I_S(i_f - i_r) \quad (11)$$

$$I_S = 2n\beta U_T^2 \quad (12)$$

$$i_f = [\ln(1 + e^{\frac{v_p - v_s}{2}})]^2 \quad (13)$$

$$i_r = [\ln(1 + e^{\frac{v_p - v_d}{2}})]^2 \quad (14)$$

where I_S is the specific current. i_f, i_r are normalized forward and reverse current, and v_p, v_s, v_d are normalized pinch off voltage, source and drain voltages [10].

The MOSFET equivalent capacitor is:

$$C_{eq} = \frac{C_{gs}C_{bs}}{C_{gs} + C_{bs}} + \frac{C_{gd}C_{bd}}{C_{gd} + C_{bd}} + C_{gb} \quad (15)$$

where $C_{gs}, C_{bs}, C_{gd}, C_{bd}, C_{gb}$ are nonlinear parameters and their definitions follow the EKV MOSFET model definitions in [10].

This decoupled MOSFET macro-models preserve the EKV MOSFET I-V and capacitor properties with a simpler structure. Therefore it is easy to combine them structurally in the digital cell noise model.

4. DIGITAL CELL MACRO-MODELS

This section discusses the derivation of macro-models for digital cells. Examples are shown for primary cells such as

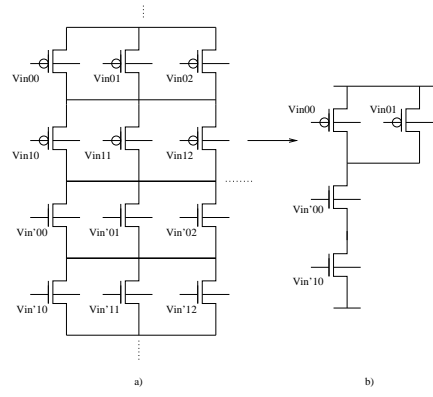


Figure 5: MOSFET array

inverter and nand2 gates. For comprehensive cells we introduce model composition and present the buffer macro-model as an example.

4.1 Symbolic equations for model derivation

For primary cells such as inverter and nand2 gate, the symbolic expression of V_{out} and V_{sub} are derived from the following nodal equations:

1. Power/GND line electrical property.

$$\widetilde{I}_{sp} = \frac{C_{pkgn}}{h}(\widetilde{V}_{sn} - \widetilde{V}_{sn0}) + \frac{\widetilde{V}_{sn} - GND - \frac{I_{Ln0}L_n}{h}}{R_{pkgn} - \frac{L_n}{h}} \quad (16)$$

$$\widetilde{I}_{sn} = \frac{C_{pkgp}}{h}(\widetilde{V}_{sp} - \widetilde{V}_{sp0}) + \frac{\widetilde{V}_{sp} - GND - \frac{I_{Lp0}L_p}{h}}{R_{pkgp} - \frac{L_p}{h}} \quad (17)$$

where $\widetilde{I}_{sp}, \widetilde{I}_{sn}$ are total current into PMOS transistors/out of NMOS transistors. $C_{pkgn}, C_{pkgp}, L_n, L_p$ refers to the parasitic coupling and h is the transient time step.

2. MOSFET connection.

In order to generate digital cell automatically, the MOSFET array M as shown in Figure 5 is used as a starting topology. The selection matrix $SELPUN, SELPDN$ are used to select the MOSFET in the pull-up network and pull-down network PUN and PDN. The composition matrix $COM(PUN), COM(PDN)$ are used to derive the MOSFET topology in PUN and PDN, as described in I(PDN/PUN). Combining I(PDN/PUN) we get the digital cell topology as a current matrix $I(Total)$, each line of the matrix describes the current flowing at one level of the topology. The nodal equations are derived from $I(Total)$ as shown in the following Nand2 topology derivation example.

As an example, for Nand gate,

$$M(PUN) = \begin{bmatrix} I_{dp00} & I_{dp01} \\ I_{dp10} & I_{dp11} \end{bmatrix} \quad (18)$$

$$M(PDN) = \begin{bmatrix} I_{dn00} & I_{dn01} \\ I_{dn10} & I_{dn11} \end{bmatrix} \quad (19)$$

$$SEL(PUN) = \begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix} \quad (20)$$

$$SEL(PDN) = \begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix} \quad (21)$$

$$COM(PUN) = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (22)$$

$$COM(PDN) = \begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix} \quad (23)$$

$$I(PUN/PDN) = M \cdot SEL \times COM(PUN/PDN) \quad (24)$$

$$I(Total) = I(PUN) \cup I(PDN) \quad (25)$$

$$= \begin{bmatrix} I_{dp00} \\ I_{dp10} \\ I_{dn00} + I_{dn10} \end{bmatrix}$$

The nodal equation for node between $MOS_{i,j}$ and $MOS_{(i+1),j}$

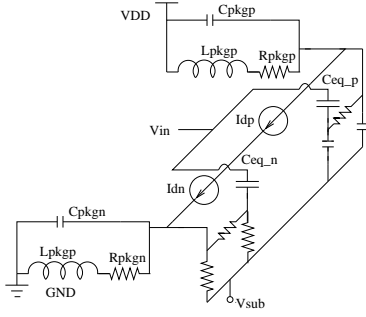


Figure 6: Inverter noise injection model

in the digital cell is:

$$\sum_{j=1,n} I(Total)_{i,j} + \sum_{j=1,n} I(Total)_{i+1,j} = 0 \quad (26)$$

3. Injection to substrate node.

$$I_{inj} = C_{eq} V_{in} - V_{in0} + V_b - V_{b0} h \quad (27)$$

where C_{eq} is the equivalent capacitance of the MOSFET. V_{in0} , V_{in} are the input voltage, and V_{b0} , V_b are the body voltage at the beginning and the end of a transient time step.

4. Substrate networking.

The equation for substrate network is described in section 3 equation (1)-(10).

4.2 Nonlinear function approximation error

The nonlinear MOSFET current model and capacitor model causes difficulties in deriving symbolic expressions for V_{out} and V_{sub} , and I_{inj} . To solve the problem we used Piece-wise Newton interpolation of the 1st and 2nd order to make V_{out} , V_{sub} , I_{inj} solvable.

The error associated with the piece-wise model include *inter segment error* and *intra segment error*. Inter-segment error refers to the difference between the piece-wise segment and the original function. By choosing small segment length (0.005) this error is controlled within 10^{-8} . *Intra-segment error* refers to the deviation from original model with an inappropriate choice of the segment. To reduce this error we search exclusively over possible segments and pick the segment that provides the closest approximation to the original nonlinear function.

4.3 Primary digital cell macro-models

The primary digital cell macro-models is a composition of the power/ground coupling, substrate coupling and MOSFET noise injection model we discussed in Section 3. Figures 6 and 7 show the macro-model of the INV and Nand2 cell as examples for primary digital cells. This section presents the symbolic equations describing the macro-model.

A. Inverter macro-model

The Inverter macro-model can be described by the following nodal equations corresponds to the important nodes in the macro-model such as input node, output node, substrate node, and power/gnd line node. The notation follows equation (17)-(28).

$$I_{dp} - I_{dn} - C_{out} \frac{dV_{out}}{h} = 0 \quad (28)$$

$$I_{dn} + I_{inj} = C_{pkgn} \frac{\widetilde{V}_{sn}}{h} + I_{Ln0} - \frac{hd\widetilde{V}_{sn}}{L_n} \quad (29)$$

$$V_{Ln}/R_{pkgn} = I_{Ln0} - h \frac{\widetilde{V}_{sn} + d\widetilde{V}_{sn} - V_{Ln}}{L_n} \quad (30)$$

$$C_{eqp} \frac{dV_{in} - d\widetilde{V}_{sp}}{h} + C_{eqn} \frac{dV_{in} - dV_{bn}}{h} = 0 \quad (31)$$

$$\frac{\widetilde{V}_{sn0} + d\widetilde{V}_{sn} - V_{sub}}{r_0} = \frac{V_{bn0} + dV_{bn} - V_{sub}}{r_1} \quad (32)$$

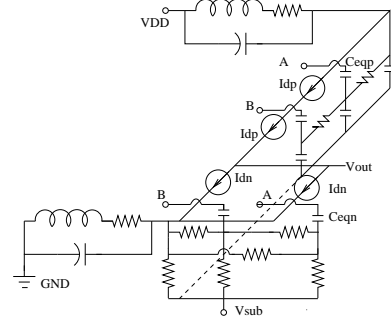


Figure 7: Nand2 noise injection model

The symbolic expression of the voltage at each input of the substrate network can be derived from these equations. The injection current I_{inj} therefore can be obtained from the substrate network template as we discussed in equation (1) and (5).

B. Nand macro-model

The Nand2 macro-model can be described by the following nodal equations corresponds to the important nodes in the macro-model such as input node, output node, substrate node, intermediate node in PDN and power/gnd line node. The notation follows equation (17)-(28), V_{node} is the voltage at the PDN intermediate node.

$$I_{dp0} + I_{dp1} - I_{dn} - C_{out} dV_{out}/h = 0 \quad (33)$$

$$I_{dn0} - I_{dn1} = C_{node} \frac{dV_{node}}{h} \quad (34)$$

$$I_{dn0} + I_{inj0} + I_{inj1} = C_{pkgn} \frac{\widetilde{V}_{sn}}{h} + I_{Ln0} - \frac{hd\widetilde{V}_{sn}}{L_n} \quad (35)$$

$$\frac{V_{Ln}}{R_{pkgn}} = I_{Ln0} - h \frac{(\widetilde{V}_{sn} + d\widetilde{V}_{sn} - V_{Ln})}{L_n} \quad (36)$$

$$C_{eqp} \frac{dV_{in} - d\widetilde{V}_{sp}}{h} + C_{eqn} \frac{dV_{in} - dV_{bn}}{h} = 0 \quad (37)$$

$$\frac{\widetilde{V}_{sn0} + d\widetilde{V}_{sn} - V_{sub}}{r_0} - \frac{\widetilde{V}_{sn0} + d\widetilde{V}_{sn} - V_{bn2}}{r_{20}} - \frac{\widetilde{V}_{sn0} + d\widetilde{V}_{sn} - V_{bn1}}{r_{10}} = \frac{V_{bn01} + dV_{bn1} - V_{sub}}{r_1} + \frac{V_{bn01} + dV_{bn1} - V_{bn00} + dV_{bn0}}{r_{10}} + \frac{V_{bn02} + dV_{bn2} - V_{sub}}{r_2} \quad (38)$$

Similar to INV cell, the symbolic expression of the voltage at each input of the substrate network can be derived from these equations. The injection current I_{inj} therefore can be obtained from the substrate network template as we discussed in equation (1) and (5).

4.4 Composed digital cell macro-model

For digital cell composed of primary cells, the noise injection model can be generated by composing the primary cell noise macro-model electrically. As an example, Figure 8 shows the macro-model a buffer cell composed by 2 inverter noise models.

The following equation describes the composition of the inverter macro-model to get the buffer model. I_{inj0} and I_{inj1} are injection current from the NMOS to the substrate and they come from the inverter noise macro-model. Similarly I_{inj0} and I_{inj1} are injection current from the PMOS to the substrate and they come from the inverter noise macro-model. The Gm matrixes in the following equations are instantiated from the substrate network template presented in equation (1) and (5) for the buffer. With these equations we can derive the body voltages of MOSFETs, as well as the substrate noise voltage V_{sub} for the buffer cell.

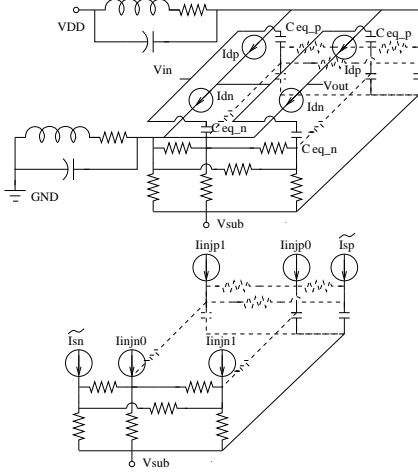


Figure 8: Buffer noise injection model

$$\begin{bmatrix} \widetilde{I}_{sn} \\ I_{injn_0} \\ I_{injn_1} \end{bmatrix} = \begin{bmatrix} \frac{-1}{r_{2,0}} & \frac{-1}{r_{1,0}} & \frac{1}{r_{2,0}} & \frac{-1}{r_0} \\ \frac{-1}{r_{2,1}} & \frac{1}{r_{2,1}} & \frac{1}{r_{1,0}} & \frac{-1}{r_1} \\ \frac{1}{r_{2,0}} & \frac{-1}{r_{2,1}} & \frac{-1}{r_{2,0}} & \frac{-1}{r_2} \\ +\frac{1}{r_{2,1}} & +\frac{1}{r_2} & & \end{bmatrix} \begin{bmatrix} V_{bn_1} \\ V_{bn_0} \\ V_{sn} \\ V_{sub} \end{bmatrix} \quad (39)$$

$$\begin{bmatrix} \widetilde{I}_{sp} \\ I_{inj_{p0}} \\ I_{inj_{p1}} \end{bmatrix} = \begin{bmatrix} \frac{-1}{r_{2,0}} & \frac{-1}{r_{1,0}} & \frac{C_0}{h} & \frac{-C_0}{h} \\ \frac{-1}{r_{2,1}} & \frac{C_1}{h} & \frac{1}{r_{2,0}} & \frac{-C_1}{h} \\ +\frac{1}{r_{2,1}} & +\frac{1}{r_{2,1}} & \frac{1}{r_{1,0}} & \\ \frac{1}{r_{2,0}} & \frac{1}{r_{2,1}} & \frac{-1}{r_{2,0}} & \frac{-C_2}{h} \\ +\frac{1}{r_{2,1}} & +\frac{C_2}{h} & & \end{bmatrix} \begin{bmatrix} V_{bp_1} \\ V_{bp_0} \\ V_{sp} \\ V_{sub} \end{bmatrix} \quad (40)$$

$$+ \begin{bmatrix} 0 & 0 & \frac{-C_0}{h} & \frac{C_0}{h} \\ 0 & \frac{-C_1}{h} & 0 & \frac{C_1}{h} \\ \frac{-C_2}{h} & 0 & 0 & \frac{C_2}{h} \end{bmatrix} \begin{bmatrix} V_{bp_{01}} \\ V_{bp_{00}} \\ V_{sp0} \\ V_{sub0} \end{bmatrix}$$

5. SIMULATION EXPERIMENTS

This section offers noise simulation results for inverter, nand2 and the buffer macro-model.

5.1 Simulation accuracy and speed up

The substrate injection noise simulation of the inverter for 333MHz digital inputs with different input peak to peak transition steps (250ps/350ps) and technology (0.25um /0.35um) was performed. The noise peaks scale with device sizes and are approximately inverse proportional to the transition time. For multiple input circuits the noise peaks are also related to the input switching combinations. Our experiment result for Nand2 in Figure 11 shows that simultaneous switching of the inputs in the same direction produces the largest injection noise V_{sub} .

Our noise macro-model offers better simulation results than models without transistors, as shown in Figure 9, because it considers the nonlinear transistor parasitic capacitors and the interactions between PMOS and NMOS during transitions.

Comparing the symbolic technique with SPICE, the difference is within 5-10%. The error control is related the inter-segment error and intra-segment error of our piece-wise approximation, as we discussed in Section 4.2. Currently we

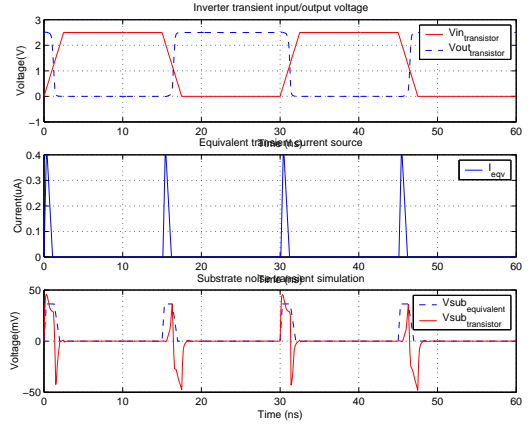


Figure 9: Noise simulation with equivalent current source tuning compared with SPICE

controlled the error with in 10^{-8} with simulation time step $h = 0.01ps \sim 0.1ps$.

Currently we achieve 4 times speed up than SPICE. Using composition of macro-model the simulation speed can be increase in a large scale. Table 1 shows that 50% of simulation time is spent on piece-wise approximation and segment selection, to improve the speed-up we will continue to study better approximation methods.

	Search for right segment	Solving expression	Symbolic (300 clk)	SPICE (300 clk)
INV	50%	50%	62sec	260sec
NAND2	50%	50%	150sec	570sec
BUF	49%	51%	75sec	330sec

Table 1: Time on approximations, symbolic expression solving, and total time(Symbolic vs. SPICE)

5.2 Scalability

Noise model composition is proposed for larger cells in order to reduce the coding effort of flat model simulation. There are three metrics to indicate the quality of composed model: *Code Reusability* ρ , *Effort saving* σ , and *Composition error* ε :

$$\rho = \frac{\text{codelength}(\text{basiccell})}{\text{codelength}(\text{secondarycell}) + \text{codelength}(\text{basiccell})} \quad (41)$$

$$\sigma = 1 - \frac{\text{codelength}(\text{secondarycell, composition})}{\text{codelength}(\text{secondarycell, scratch})} \quad (42)$$

Composition Error ε is related to the basic cell error and the substrate parasitics. A buffer example is used to illustrate ε . Good composition quality requires $\rho, \sigma \rightarrow 1$ and $\varepsilon \rightarrow 0$.

The buffer noise model is composed of two symbolic INV noise injection model. Composition follows the electrical property of the buffer substrate template, as shown in Figure 8. For our experiments we have ≈ 2000 , $\rho = 0.95$ and $\sigma = 0.9525$, which shows that code reusability was very high and modeling effort for buffer was largely saved.

Simulation accuracy is within 10% compared to SPICE simulation, as shown in Figure 12. The source of the error ε_{BUF} comes from the error ε_{INV} of the inverter module (capacitors in PMOS substrates negligible from layout extraction):

$$\varepsilon_{BUF} = \frac{(\varepsilon_{INV1}r_{n_{2,1}}r_{n_1}r_{n_{2,0}}r_{n_2} - \varepsilon_{INV2}r_{n_{1,0}}r_{n_2}r_{n_{2,1}}r_{n_1})}{r_{n_{2,1}}(r_{n_{1,0}}r_{n_2} - r_{n_{2,0}}r_{n_1})}; \quad (43)$$

ε_{INV1} and ε_{INV2} are different at each time step because the transition is reversed. For the buffer template with $r_{n_{1,0}} \approx r_{n_{2,0}}$ (results from layout extraction):

$$\varepsilon_{BUF} \in [0, \max(2\varepsilon_{INV1}, 2\varepsilon_{INV2})] \quad (44)$$

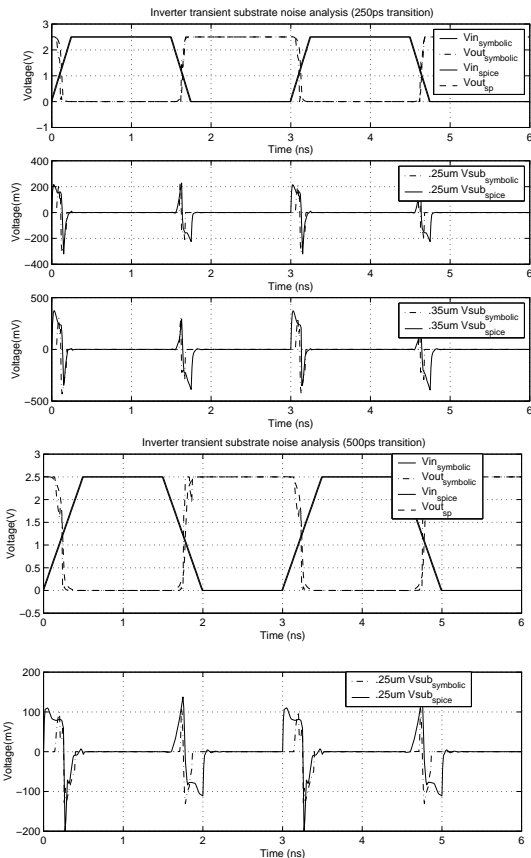


Figure 10: Inverter substrate noise for 250ps/500ps transition time on 0.25um and 0.35um technology

In general, noise model composition saves significant effort in developing noise model for larger digital circuit without losing much accuracy provided that good control of simulation error exists for basic digital cells. The method is potentially capable of handling large scale digital circuits by hierarchically building noise models. Since the spacial information of the substrate injection point is incorporated in the substrate network template. Using this modelling method we are able to predict the spatially and temporally the occurrence of substrate noise peaks in a digital design.

6. CONCLUSION

In this paper we proposed a substrate noise macro-model for digital cell with a substrate template and an equivalent EKV MOSFET model. Symbolic expressions are derived for the substrate voltage, injection current and output voltage of each primary digital cells. Proposed models contain physical detail of the device and process, therefore they are valid for different processing technology and input transition, and are more accurate as compared to the macro-model generated from Spice simulation and curve fitting. Our macro-models are accurate within 5-10% from SPICE simulation with the full circuit and MOSFET model, and the simulations are at least 4 times faster. The method has potentials to predict temporally and spatially the occurrence of substrate noise peaks for large digital design using macro-models composed of primary digital cell models.

7. REFERENCES

- [1] M. Badaroglu *et al.*, "High-Level Simulation of Substrate Noise Generation from Large Digital Circuits with multiple Supplies", *Proc. DATE*, 2001, pp. 326-330.
- [2] R. Murgai *et al.*, "Sensitivity-based Modeling and Methodology For Full-Chip Substrate Noise Analysis", *Proc. DATE*, 2004.

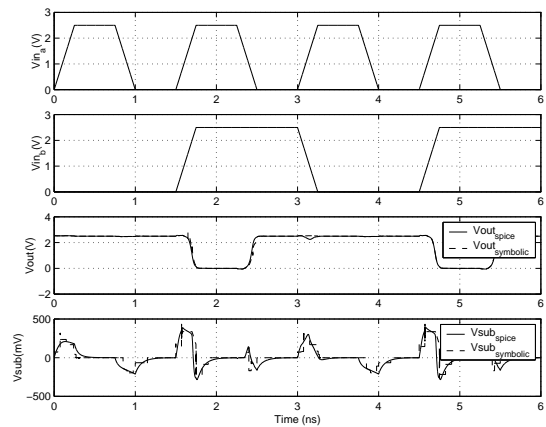


Figure 11: nand2 substrate noise simulation result

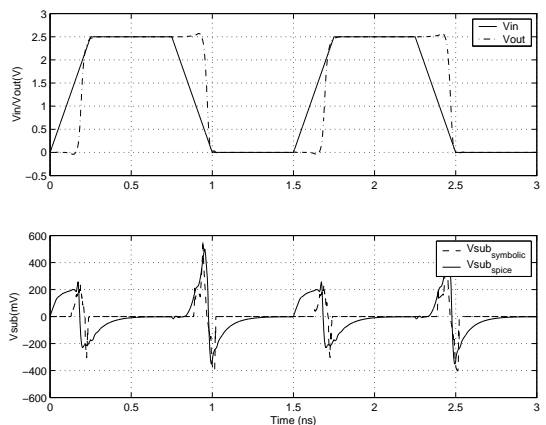


Figure 12: Buffer substrate noise simulation result

- [3] A. Samavedam *et al.*, "A Scalabel Substrate Noise Coupling Model for Design of Mixed-Signal IC's", *JSSC*, Vol.35, No. 6, June 2000.
- [4] J. Briaire, K. S. Krish, "Principles of Substrate Crosstalk Generation in CMOS circuits", *IEEE Trans. CAD*, Vol. 18, No.6, June 2000, pp. 645-653.
- [5] A. Koyama *et al.*, "Switching Well Noise Modeling and Minimization Strategy for Digital Circuits with a Controllable Threshold Voltage Scheme", *IEEE Trans. CAD*, Vol.19, No.6, June 2000, pp. 654-670.
- [6] X. Aragonés *et al.*, "Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs", *Kluwer*, 1999.
- [7] N.P. van der Meijs *et al.*, *SPACE USER's Manual*, May 2003.
- [8] N. K. Verghese *et al.*, "Rapid Simulation of Substrate Coupling Effects in Mixed-model ICs", *Proc. CICC*, 1993, pp. 18.3.1-18.3.4.
- [9] R. Gharpurey *et al.*, "Modeling and Analysis of Substrate coupling in integrated circuits", *Journal of Solid-state Circuits*, Vol. 31, No.3, March 1996.
- [10] C. Enz *et al.*, "An analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", *Analog Integrated Circuits and Signal Processing*, Kluwer, 1995.
- [11] L. P. Huelsman, "Personal computer symbolic analysis programs for undergraduate engineering courses", *Proc. ISCAS*, 1989, pp. 798-801.
- [12] D. Foty, "MOSFET modeling with Spice", *Prentice Hall*, 1997.
- [13] Tanner Consulting and Engineering Services, "Digital Low Power Standard Cell Library".
- [14] Removed for blind review.