ACTIVE SPATIAL FILTERING FOR A/D CONVERTERS

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ABSTRACT

A technique of offset averaging for reducing INL and DNL in flash and folding A/D converters is presented in this paper. The proposed method uses second-order active resistive networks implementing gaussian-like spatial filters. Compared to previously reported methods employing passive resistive grids, a better offset reduction is achieved without sacrificing the signal gain. Both behavioral and transistor-level simulation results confirmed the performance of the proposed technique.

1. INTRODUCTION

Device mismatch limits the INL and DNL in standard design architecture for flash and folding A/D converters and it is a fundamental drawback in making high-resolution converters. Wider resistors in the reference ladder and larger transistors in the input preamplifiers will improve precision, but at the cost of increased die size, power dissipation and decreased sample rate. An efficient method to reduce integral and differential nonlinearity errors in full-flash A/D converters was firstly introduced in [1]. Lateral resistors have been inserted between preamplifiers in adjacent comparator cells to average the offsets (Fig. 1). As a result, smaller size devices can be used in the input stages, increasing the operating frequency of the converter for the same DNL error. Because the tolerance of the averaging resistors is not critical for the functioning of the averaging mechanism, they can be minimum-width and do not contribute significantly to die area.

Later, this technique has been extended to A/D converters using folding and interpolation [2], [3]. In these references the lateral resistors are connected between adjacent folding amplifiers. In [3] active loads replace the passive output resistors R_0 in Fig. 1 and the lateral resistors are connected in a cyclic manner between all folding amplifiers. A more detailed analysis of the averaging mechanism has been done in [4] by viewing it as a spatial filtering. In section 2 we review the theoretical foundation of resistive averaging networks and in section 3 we show that higher-order spatial filters are needed to increase the efficiency of the method. Section 4 is dedicated to simulation results and circuit implementation. Throughout this communication we will refer mainly to the case of folding amplifiers, but similar results can be obtained for the case of simple preamplifiers.

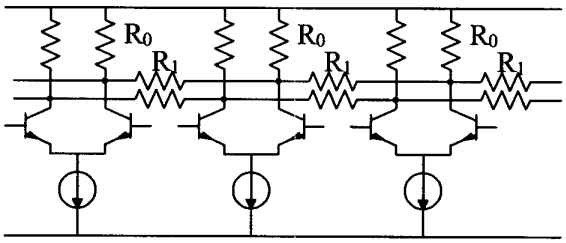

Figure 1. Passive resistor network for offset averaging

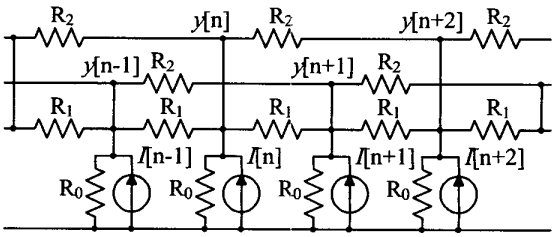

Figure 2. Resistive spatial filter

2. RESISTIVE GRIDS AS SPATIAL FILTERS

In the past years resistive networks, both linear and nonlinear, have attracted a lot of attention as image processing tools [6]-[8]. Such one-dimensional spatial filter is depicted in Fig. 2. The current sources $I[n]$, represent the inputs, whereas the node voltages $y[n]$ are the outputs. The resistor indexes show how many nodes the corresponding resistor spans. Obviously, the network shown in Fig. 2 can be generalized to 2D and to higher-orders (resistors spanning more than 2 nodes)

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as well. For the purpose of our intended application, the one-dimensional resistive grid in Fig. 2 will suffice.

Comparing the offset-averaging technique in Fig. 1 and the resistive spatial filter in Fig. 2, one can easily see that they are equivalent, the circuit in Fig. 1 implementing a spatial filter containing only resistors spanning a single node and being described by the equation

$$y[n] = a(y[n-1] + y[n+1]) + (1-2a)x[n], \quad (1)$$

where

$$a = \frac{R_0}{R_1 + 2R_0} \quad (2)$$

and $x[n] = R_0 I[n]$ are the node voltages if the lateral resistors are not present. Eq. (1) describes a first-order non-causal IIR filter that is stable for $|a| < 0.5$ and with a frequency response given by

$$H(\omega) = \frac{1-2a}{1-2a\cos\omega} \quad (3)$$

For $0 < a < 0.5$ one obtains a low-pass filter. The bandwidth is set by the parameter a, the closer this parameter to 0.5, the narrower the filter.

A first-order resistive network with nearest-neighbor connections produce only an exponential convolution, equivalent to a poor selectivity in the frequency domain. Hence, extension to higher orders are needed in practice. The network shown in Fig. 2 is described by the difference equation

$$\begin{aligned} y[n] &= a(y[n-1] + y[n+1]) + b(y[n-2] + \\ &\quad + y[n+2]) + (1-2a-2b)x[n], \end{aligned} \quad (4)$$

where

$$\begin{aligned} a &= \frac{R_0}{R_1 || R_2 + 2R_0} \frac{R_2}{R_1 + R_2} \\ b &= \frac{R_0}{R_1 || R_2 + 2R_0} \frac{R_1}{R_1 + R_2} \end{aligned} \quad (5)$$

and $x[n] = R_0 I[n]$ represent again the node voltages when the lateral resistors are not present. In spatial frequency domain one has

$$H(\omega) = \frac{1-2a-2b}{1-2a\cos\omega - 2b\cos 2\omega}. \quad (6)$$

Such a filter is expected to have a higher roll-off slope in the stop-band and therefore to implement a more efficient low-pass filter. Furthermore, two design parameters are available.

3. RESISTIVE NETWORKS FOR OFFSET AVERAGING

Folding A/D converters realize an optimum balance between power dissipation, clock frequency and die area due to the number of reduced comparators as oposed to full-flash ADCs. A folding architecture uses parallelism to enable subranging of the signal with nonlinear folding. Stringent demands on transistor matching are required, the offsets in the input folding stages limiting the linearity of the ADC.

A fully differential MOS implementation of a fold-by-four circuit is depicted in Fig. 3. An array of folding amplifiers is needed to generate M folding signals with $N \times M$ zero-crossings, where N is the folding rate. Extending the results from [4], for a given input voltage the outputs of the M folding amplifiers are:

$$v_o[n] = R_0 \left(G_f[n] v_{in} + G_f[n] v_{off}[n] + \Delta I_{tail}[n] \right) \quad (7)$$

where $G_f[n]$ represents the folding transconductance of the n^{th} amplifier, $v_{off}[n]$ is its offset, and ΔI_{tail} represents an error due to the mismatches in the tail currents. These errors behave like a "spatial noise", altering the zero crossings of the folding amplifier transfer characteristic and they should be minimized.

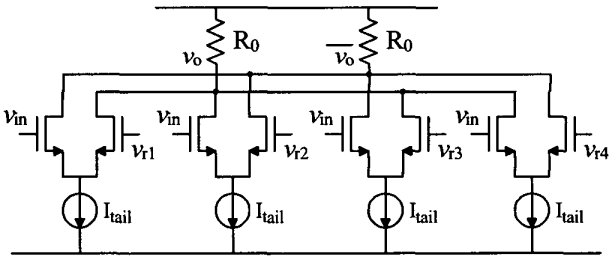

Figure 3. MOS folding amplifier

Using the same idea as in [1], several authors reported improvements in INL and DNL of the folding ADCs by connecting the neighboring outputs of the folding amplifiers [2], [3], or of the individual preamps [5] with lateral averaging resistors. As shown above, this corresponds to a spatial low-pass filtering of the output voltages in order to remove the "spatial noise" as much as possible. Assuming v_{off} and ΔI_{tail} have a flat power spectrum density, to minimize the output errors, the bandwidth of the spatial filter should be equal to the width of the main lobe of the spectrum of $G_f[n]$ and the attenuation in the stop-band to be as large as possible. However, the offsets $v_{off}[n]$ are convolved in the spatial frequency domain with the spectrum of $G_f[n]$ and thus, its output error component is not white anymore. This reduces the amount

of achievable improvement. In [3] it is claimed that by making the spatial filter narrower ($a \rightarrow 0.5$, equivalent to $R_0 \gg R_1$) one can to reduce the errors as much as one wants, being limited only by the number of preamps or folding amplifiers operating in the linear region at one instant. However, as shown in [2] and [4], since the spatial filter affects the folded signal as well, by narrowing the filter bandwidth too much, the amplitude of the folded signal is also decreased and SNR is actually worsened.

The limits of the first-order resistive network and its optimum design are discussed in [4]. To improve furthermore the INL and DNL of the folding ADCs by using resistive averaging, higher-order resistive grids are needed. The first step into this direction is to use second-order passive networks, characterized by a frequency response (6) with $a, b > 0$. However, this approach does not bring any additional improvement in DNL and INL compared to first-order resistive grids because of the dissipative nature of the filter that restricts the location of its poles to the real axis. It was shown in [7] that one can obtain a Gaussian-like frequency response with second-order resistive networks if $b < 0$ and $|b| = a/4$. In terms of circuit elements, this is equivalent to using a negative resistor R_2 having its absolute value equal to $4R_1$. The bandwidth of the resulting active filter is set by the R_0/R_1 ratio. Such a filter has a flatter frequency response in the pass-band and a higher attenuation in the stop-band compared to passive resistive networks (see Fig. 4) and achieves better offset reduction, as shown in the next section.

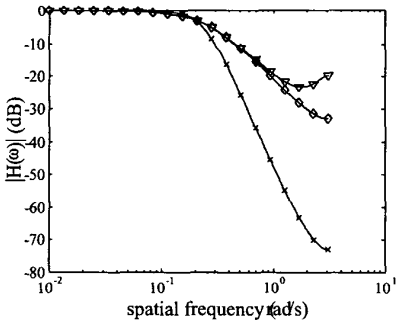

Figure 4. Spatial frequency response of three resistive networks. $\diamond$ first-order network; ∇ second-order passive network ($a = b$); $\times$ second-order active network (gaussian).

4. SIMULATION RESULTS AND CIRCUIT IMPLEMENTATION

Numerous computer simulations have been run to verify the above theoretical claims. The obtained results, both from behavioral simulations in Matlab and from transistor level simulations in Spice, confirmed the fact that the second-order active resistive networks achieve better DNL improvement compared to their passive counterparts. Fig. 5 shows the average DNL improvement for a folding-by-5 stage with 16 folding signals as a function of the -3dB spatial bandwidth of the resistive averaging filter. The erroneous zero-crossings of the dummy stages have been eliminated from the presented results. On the same graph the amplitude of the output folding signals, normalized to $R_0 I_{tail}$, is plotted. One can see that for small bandwidths, the signal amplitude is drastically decreased and the true error correction factor (ECF) should consider this effect by multiplying the obtained improvement by the signal gain. Figures 6 and 7 show the INL and DNL ECFs, respectively, for the three types of resistive averaging networks. The improvement in DNL is more than two times larger when using the gaussian-type active filter compared to passive resistive networks. The practical improvement could be even better because the results depicted in figures 5-7 have been obtained without considering the ΔI_{tail} term from Eq. (7).

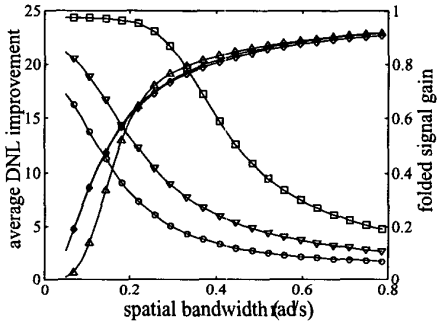

Figure 5. DNL improvement for: ∇ - first-order network; o - second-order passive network; $\square$ - active gaussian network. Signal gain: $\diamond$ - first-order network; $\times$ - second-order passive network; $\triangle$ - active gaussian network.

The behavior of the second-order active resitive averaging network has been tested at the circuit level as well. The negative resistive strings have been implemented using differential Negative Impedance Converters NIC (Fig. 8), part of the resulting folding stage being depicted in Fig. 9. The results obtained by simulating the fold-by-5 stage with 16 folding signals are similar to the ones from Matlab. At a first sight, it seems that the additional NICs will increase the die area and power consumption. However, the decrease in the size of the transistors in the folding amplifiers is four times larger compared to the passive network approach. The NIC transistors can be minimum size because their matching is not important and the additional resistive grids can be minimum-width. Furthermore, the active resistive network increases the gain of

the folding amplifiers and therefore their tail currents can be reduced.

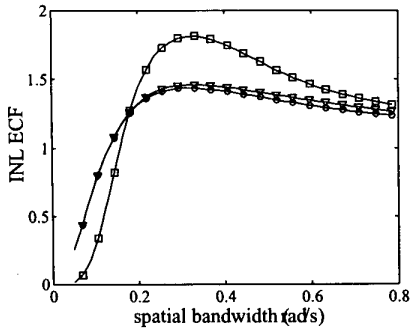

Figure 6. True INL improvement for: ▽ - first-order network; ○ - second-order passive network; □ - active gaussian network.

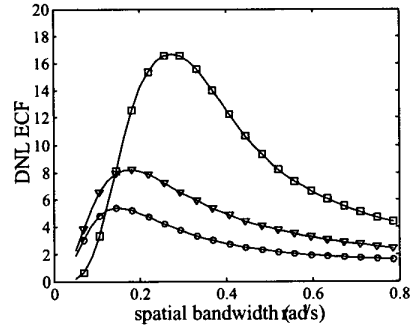

Figure 7. True DNL improvement for: ▽ - first-order network; ○ - second-order passive network; □ - active gaussian network.

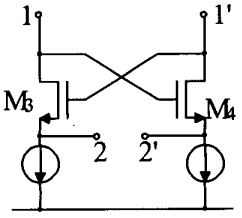

Figure 8. MOS differential negative impedance converter (NIC)

5. CONCLUSIONS

A second-order active resistive averaging approach for achieving higher DNL improvement in full-flash and folding A/D converters is presented in this communication. The spatial filter employs negative resistors that are implemented using fully differential negative impedance converters. The achievable DNL improvement in the case of a folding-by-5 stage with 16 folding signals is more than 2 times larger compared to classical passive approach, without significantly increasing the power consumption and die area. The proposed technique will increase both the resolution and the speed of the A/D converters, final results to be presented elsewhere.

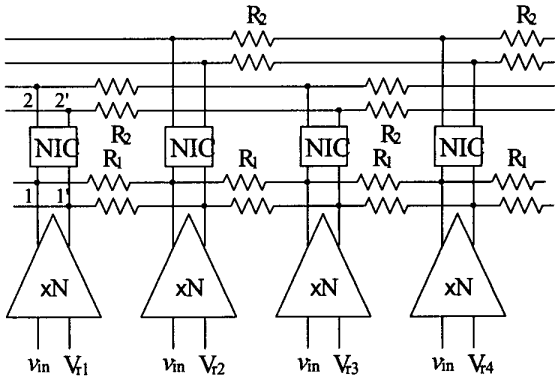

Figure 9. Active resistive offset averaging for a folding A/D converter

6. REFERENCES

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