# A HIGHLY LINEAR LOW-VOLTAGE MOS TRANSCONDUCTOR

Adrian Leuciuc and Yi Zhang

State University of New York at Stony Brook
Department of Electrical and Computer Engineering
Stony Brook, NY 11794, USA

## ABSTRACT

This paper presents a new linear MOS transconductor consisting of a differential pair with resistive source degeneration and an extra pair of op-amps to increase the linearity. The proposed transconductor operates at a 1.8V supply voltage and the achieved THD is better than -80dB up to 2.5MHz for a 0.8Vp-p input differential voltage.

## 1. INTRODUCTION

The transconductor is a basic building block in analog circuit applications, such as continuous-time filters and delta-sigma modulators. Especially in the case of delta-sigma modulators for high resolution A/D converters one needs highly linear transconductors to satisfy the required signal-to-(noise+distortions) ratio. Several techniques have been proposed in the literature to improve the linearity performance of both bipolar and MOS transconductors. In the following we will refer mainly to MOS transconductors. The reported transistor-only linearization methods include: cross-coupling of multiple differential pairs [1], [2], [3], adaptive biasing [1], [4], source degeneration using MOS transistors [5], [6], shift level biasing [7], series connection of multiple differential pairs [8], and pseudo-differential stages (using transistors in the triode region or in saturation) [9], [10]. However, due to the inherent nonlinearity of transistors, reported transconductor linearity is limited to 40-60 dB. Much better linearity performance can be achieved by using resistor-based transconductors [11]-[15]. This paper describes the implementation of a highly linear resistor-based transconductor capable of low-voltage operation.

This work has been supported by the NSF Center for the Design of Analog/Digital Integrated Circuits (CDADIC).

## 2. LINEAR MOS TRANSCONDUCTORS USING RESISTIVE SOURCE DEGENERATION

Most of the resistor-based linear transconductors are based on the simple differential-pair with resistive source degeneration (Fig. 1). Using the simple quadratic equation describing the operation of MOS transistors in strong inversion, the analysis of the circuit in Fig. 1 yields:

$$v_i - Ri_o = V_{GSeff}\left(\sqrt{1+\frac{i_o}{I_0}} - \sqrt{1-\frac{i_o}{I_0}}\right) \qquad (1)$$

where $V_{GSeff}$ represents the effective gate-to-source voltage of transistors $M_1 - M_2$ and $v_i = v_{i1} - v_{i2}$. The right side term in (1), equal to the difference between the gate-to-source voltages of the two differential transistors, characterizes the nonlinearity of the transfer characteristic. It can be seen immediately that the linearity of the transconductor in Fig. 1 can be improved by either reducing $V_{GSeff}$ and/or by decreasing the ratio $i_o/I_0$. Reducing $V_{GSeff}$ below a certain level will increase the noise and reduce the bandwidth of the circuit because the transistors will operate in moderate or even weak inversion. The latter approach will increase the power consumption for a given output dynamic range.

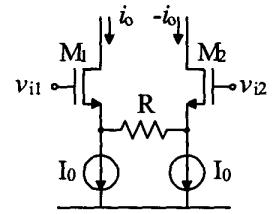


Figure 1. The differential MOS pair with resistive source degeneration.

An effective method to improve the linearity of the differential pair with resistive degeneration has been reported in [11]. Constant drain current transistors are used in the differential pair and the output current is

collected by current mirrors connected at the sources of the differential transistors. Another approach is reported in [14], but the circuit therein makes use of several current mirrors that can drastically reduce the bandwidth. The transconductor presented in [15] uses additional resistors connected in series with the inputs of the main differential pair in order to reduce the effective input voltage and improve the linearity. This circuit lacks the infinite input resistance required by most applications.

## 3. THE PROPOSED MOS TRANSCONDUCTOR

The nonlinearity of the MOS differential pair with resistive source degeneration can be eliminated if the input voltage falls entirely on the degeneration resistor. To achieve this, two additional op-amps can be connected at the inputs of the transconductor, as it is shown in Fig. 2. With ideal op-amps the above requirement is obviously satisfied and the transconductance of the circuit is $G_m = 1/R$. Considering finite gain op-amps, the analysis of the circuit yields the following $i-v$ transfer characteristic:

$$v_i - \frac{A+1}{A} R i_o = \frac{V_{GSeff}}{A}\left(\sqrt{1+\frac{i_o}{I_o}} - \sqrt{1-\frac{i_o}{I_0}}\right) \quad (2)$$

where $A$ is the gain of op-amps. This approach has been initially proposed in [12] where two simple differential pairs with single-ended outputs replace the op-amps in Fig. 2. Because no voltage level-shifting has been used, this circuit cannot operate in a low voltage environment. The circuits we propose eliminate this disadvantage as it will be shown later.

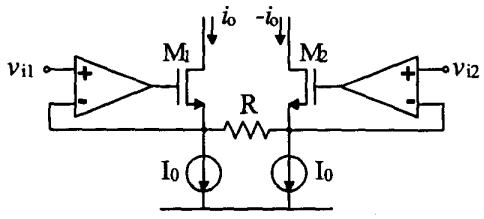


Figure 2. The proposed transconductor topology.

Before presenting the implementation issues, one question to be answered to is the needed value for the gain $A$ to achieve a desired linearity. The answer is of utmost importance because the bandwidth in which the linearity of the overall transconductor is preserved will be set by the bandwidth of the op-amps. For the same circuit complexity and power dissipation, the smaller the required gain, the larger the bandwidth will be. Starting from (2) and using the harmonic balance method when only the third harmonic is present, we obtain

$$HD_3 = \frac{I_3}{I_1} \approx \frac{1}{32A} \cdot \frac{V_{GSeff}}{RI_0} \cdot \left(\frac{V_i}{RI_0}\right)^2 \quad (3)$$

where $I_1$ and $I_3$ are the fundamental and the third harmonic of the output current, respectively, and $V_i$ is the amplitude of the input sinusoidal voltage. For example, for $V_{GSeff}$=100mV and $RI_0$=1V, to obtain $HD_3$<-80dB at $V_i$=0.8V we need $A$>21.25. The simulated THD for a circuit with the topology shown in Fig. 2 is depicted in Fig. 3. From this plot one can see that the gain of the op-amps need to be larger than the one predicted by (3). This is due to the fact that higher order harmonics contribute to THD and (3) is only an approximate expression obtained by using the simple quadratic model for the MOS transistor in strong inversion. However, the error between the simulated and predicted values of THD is only of 6-7dB.

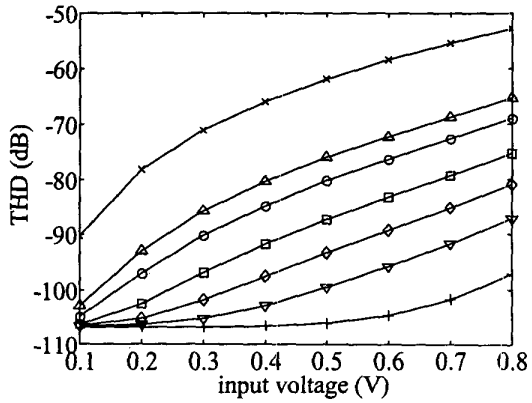


Figure 3. The simulated THD of the transconductor in Fig.2 with R=4kΩ, $I_0$=250μA, and $V_{GSeff}$=0.1V for different op-amp gains: × no amps; △ $A$=10; ○ $A$=20; □ $A$=50; ◇ $A$=100; ▽ $A$=200; + $A$=500.

## 4. CIRCUIT IMPLEMENTATION AND SIMULATION RESULTS

As mentioned before, the basic topology depicted in Fig. 2 has been originally introduced in [12]. In this reference the solution chosen for implementing the input op-amps restricts the dynamic range of the transconductor. In the following we propose two new solutions that allow the low-voltage operation of the circuit.

The first approach uses the initial configuration introduced in [12] with an additional voltage level-shifting stage. The obtained circuit is shown in Fig. 4(a). Without the level shifting circuitry ($M_{11}-M_{12}$, $M_{17}-M_{18}$), the minimum supply voltage guaranteeing the correct operation of the circuit is equal to $2V_{GS}$ +

$2V_{DS(sat)}$. The additional four transistors decrease the value of the minimum supply voltage to $V_{GS}+2V_{DS(sat)}$. The paid price is a small increase in die area and power consumption.

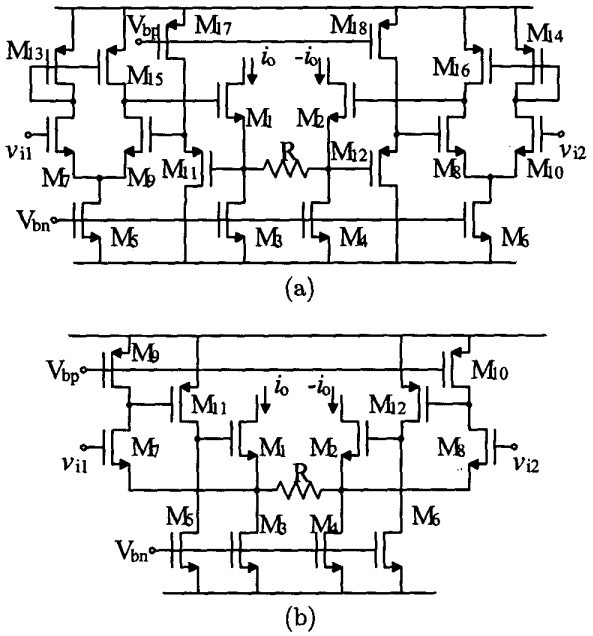


Figure 4. Two possible implementations of the transconductor in Fig. 2.

The second solution is depicted in Fig. 4(b). The two op-amps are implemented using single transistor stages $M_7$, respectively $M_8$, with active loads $M_9 - M_{10}$. Additional inverting stages $M_{11}$, $M_{12}$, are needed to obtain the negative feedback. It is easy to check that the minimum required supply voltage is $V_{GS} + 2V_{DS(sat)}$, the same as in the case of the circuit in Fig. 4(a). Because the necessary gain to achieve distortions lower than -80dB is small and it can be obtained with a single stage amplifier, in the final realization of the circuit in Fig. 4(b), transistors $M_5 - M_6$ (the loads for the second stages of the op-amps) are connected as diodes. This way one can easily obtain gains in the range of 40dB and bandwidths up to several tens of MHz.

The circuits in Fig. 4 have been designed using the TSMC CMOS $0.25\mu m$ process and a single 1.8V supply voltage, and simulated in Hspice. The presented simulation results are for the circuit in Fig. 4(b). Figure 5 shows the simulated transconductance for different source degeneration resistor values. In Fig. 6 the simulated THD as a function of the input signal amplitude and frequency is plotted. THD is less than -80dB for a 0.8Vp-p up to 2.5MHz and with R=3kΩ. Figure 7 shows the simulated total input referred noise voltage obtained when considering both thermal and flicker noise generators of the MOS transistors (1/f noise parameters supplied by TSMC). Total equivalent input referred noise voltage is around $30\mu$V at 2.5 MHz for R=3kΩ.

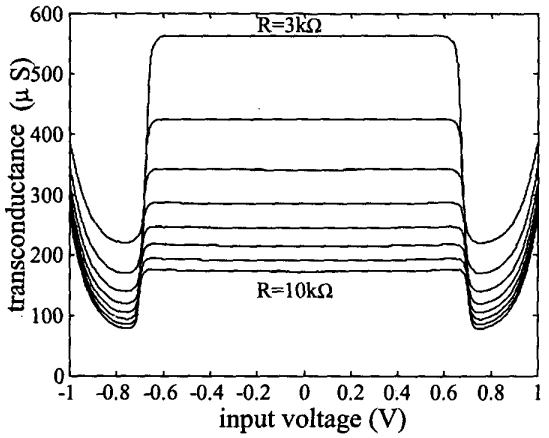


Figure 5. The simulated transconductance for different values of the source resistor.

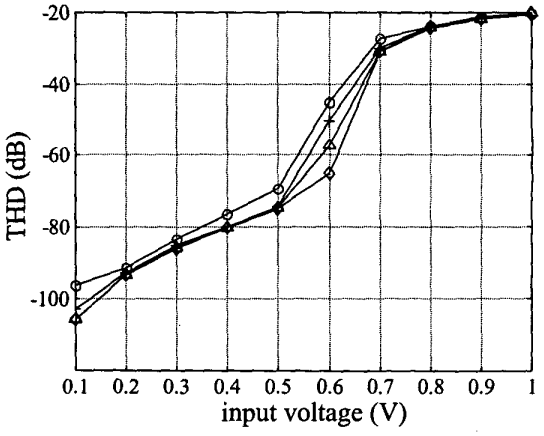


Figure 6. Simulated THD for different frequencies: ◇ 100kHz; △ 1MHz; ○ 2.5MHz; + 5MHz.

## 5. CONCLUSIONS

A highly linear transconductor consisting of a MOS differential pair with resistive source degeneration and an extra pair of op-amps boosting its linearity is presented. A very simple and effective implementation of the supplementary op-amps ensures the operation of the transconductor at low-supply voltages. The circuit can be used in continuous-time filters with tough linearity requirements or in high SNDR continuous-time delta-sigma modulators. Tuning can be achieved by means of resistive arrays or by using electronically controlled current mirrors.

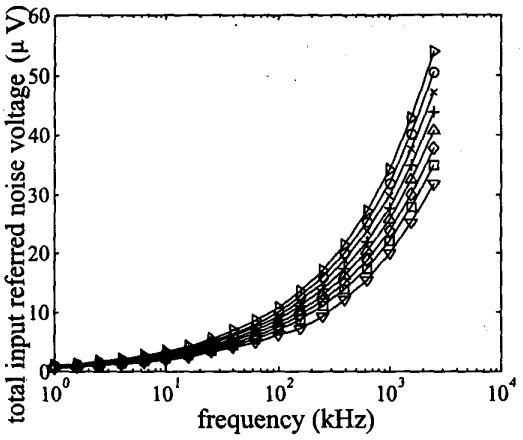


Figure 7. Simulated noise performance for different degeneration resistor values: ▽ 3kΩ; □ 4kΩ; ◇ 5kΩ; △ 6kΩ; + 7kΩ; × 8kΩ; ○ 9kΩ; ▷ 10kΩ.

## 6. REFERENCES


[1] A. Nedungadi and T. R. Viswanathan, "Design of Linear CMOS Transconductance Elements," IEEE Trans. Circuits and Systems, vol. CAS-31, No. 10, pp.891-894, Oct. 1984.

[2] H. Khorramabadi, "High frequency CMOS continuous time filter," PhD dissertation, University of California, Berkeley, 1985.

[3] E. Seevinck and R.F. Wassenaar, "A versatile CMOS linear transconductor/square-law function circuit," IEEE J. Solid-State Circuits, vol. SC-22, pp. 366-377, June 1987.

[4] M.G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. De Man, "Adaptive biasing CMOS amplifiers," IEEE J. Solid-State Circuits, vol. SC-17, pp.522-528, June 1982.

[5] F. Krummenacher and N. Joehl, "A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," IEEE J. of Solid-State Circuits, vol. SC-23, no.3, pp.750-758, June 1988.

[6] I. Mehr and D.R. Welland, "A CMOS continuous-time $G_m - C$ filter for PRML read channel applications at 150Mb/s and beyond," IEEE J. Solid-State Circuits, vol. SC-32, pp. 499-513, April 1997.

[7] Z. Wang and W. Guggenbuhl, "A voltage-controlled linear MOS transconductor using bias offset technique," IEEE J. Solid-State Circuits, vol. SC-25, pp. 315-317, Feb. 1990.

[8] J. Silva-Martinez, M.S.J. Steyaert, and W. Sansen, "A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning," IEEE J. Solid-State Circuits, vol. SC-27, pp. 1843-1853, Dec. 1992.

[9] R. Alini, A. Baschirotto, and R. Castello, "Tunable BiCMOS continuous-time filter for high-frequency applications," IEEE J. Solid-State Circuits, vol. SC-27, pp. 1905-1915, Dec. 1992.

[10] S.L. Wong, "Novel drain-based transconductance building blocks for continuous-time filter applications," Electron. Lett., vol. 25, no. 2, pp.100-101, Jan. 1989.

[11] D.R. Welland, "Transconductance amplifiers and exponential variable gain using the same," U.S. Patent 5 451 901, Sept. 19, 1995.

[12] Z.Y. Chang, D. Haspelagh, and J. Verfaillie, "A highly linear CMOS $G_m$-C bandpass filter with on-chip automatic tuning," IEEE J. Solid-State Circuits, vol. SC-32, pp. 388-397, March 1997.

[13] K. Kimura, "A linear transconductance amplifier obtained by realizing a floating resistor," IEEE Trans. Circuits and Systems - I, vol. CSI-45, pp. 108-113, Jan. 1998.

[14] E.K.F. Lee, "Low-voltage opamp design and differential difference amplifier using linear transconductor with resistor input," IEEE Trans. Circuits and Systems - II, vol. CSII-47, pp. 776-778, Aug. 2000.

[15] U. Chilakapati, T. Fiez, and A. Eshraghi, "A 3.3V transconductor in 0.35$\mu$m CMOS with 80dB SFDR up to 10MHz," Proc. of CICC 2001, May 2001, pp. 459-462.