A Novel Linear Tunable MOS Transconductor

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***Abstract*—This paper presents a new configuration for linear MOS voltage-to-current converters (transconductors). The proposed circuit combines two previously reported linearization methods [1], [2]. The novel topology exhibits very good linearity for both balanced and unbalanced inputs. The linearity is preserved during the tuning process for a moderate range of transconductance values.**

I. Introduction

Integrated analog filters can be realized using two different approaches: discrete-time (switched-capacitor or switched-current) and continuous-time implementations. The switched-capacitor and switched-current filters are limited to low frequency signals due to their clock rate needed to be greater than twice the signal bandwidth. The continuous-time filters, on the other hand, have a significant speed advantage over discrete-time counterparts because no sampling is required.

There are three main techniques to implement continuous-time filters: active RC, MOSFET-C, and G_m-C. The active RC configurations have good linearity if linear resistors and capacitors are available. However, they require large die area for resistors and/or capacitors. The large value resistors can introduce substantial thermal noise. MOSFET-C implementations have the advantage of tuning capability. Nevertheless, they have poor linearity due to nonlinear characteristic of the input MOS transistors functioning in the triode region. Although the linearity can be improved by using multiple cross-coupled transistors, the input dynamic range is reduced in order to keep the MOSFETs in the triode region. The G_m-C configurations have a better frequency response compared to active-RC and MOSFET-C realizations due to their feed-forward topology, have tuning capability, but rather poor linearity. Therefore, additional circuitry is needed to linearize the transfer characteristic of transconductor.

Since G_m-C configurations have better frequency response and usually wider tuning range, they are nowadays the most popular realizations for integrated continuous-time filters. Several circuit techniques have been proposed in literature to improve the linearity of bipolar and MOS transconductors. In this communication we will refer only to MOS transconductors. The reported linearization techniques include: cross-coupling of multiple differential pairs, adaptive biasing, source degeneration (using resistors or MOS transistors), shift level biasing, series connection of multiple differential pairs, and pseudo-differential stages (using transistors in the triode region or in saturation). This paper presents an improved linear MOS transconductor which uses both the adaptive biasing and source degeneration approaches. Section 2 reviews these two linearization techniques and the configuration of the newly proposed transconductor is described. Several comparative simulation results are presented in section 3 together with some final conclusions.

II. Circuit topologies for linear MOS transconductors

In this section, we will firstly review two linearization techniques, previously reported in literature. The first one was introduced in [1] and uses a MOS differential pair with source degeneration using triode transistors. The second one [2] makes use of an adaptive biasing current source to cancel the nonlinearity of the simple MOS differential pair. The advantages and disadvantages of these two techniques will be discussed. Then the novel linear MOS transconductor is presented.

A. MOS transconductors using source degeneration resistors implemented with MOS transistors in the triode region

Considering quadratic $i-v$ characteristics for the MOS transistors and neglecting the channel length modulation effect, the simple differential MOS transconductor (shown in Fig.1) has a transfer characteristic given by

$$\begin{aligned} i_o &= \sqrt{2\beta I_0}v_i\sqrt{1-\frac{v_i{}^2\beta}{8I_0}} \\ &= \sqrt{2\beta I_0}v_i\sqrt{1-\frac{v_i{}^2}{4(V_{GS}-V_T)^2}} \end{aligned} \tag{1}$$

where β is the transconductance parameter and V_T is the threshold voltage. Better linearity can be achieved for

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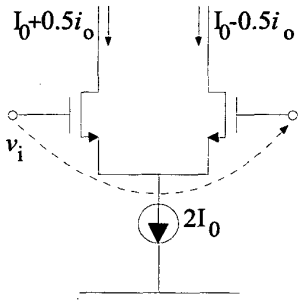

Fig. 1. The simple differential MOS transconductor

large effective gate-to-source voltages, $V_{GS_{eff}} = V_{GS} - V_T$. For low-voltage applications this constitutes a major drawback. Furthermore, large transconductance values can be obtained only by using important bias currents and large area transistors, that is area and power expensive circuits.

One of the simplest topologies to linearize the transfer characteristic of the MOS transconductor is the one using source degeneration resistors. However, this technique eliminates the electronic tuning capability of the transconductor because the transconductance value is set by the degeneration resistors. Replacing the degeneration resistors by MOS transistors functioning in the triode region the circuit in Fig.2 is obtained. Considering perfectly matched transistors and neglecting the body and channel length modulation effects, the transfer characteristic of this transconductor is given by

$$i_o = \frac{4\beta_3\sqrt{2\beta_1 I_0}}{\beta_1 + 4\beta_3} v_i \sqrt{1 - \frac{2{v_i}^2\beta_1\beta_3^2}{I_0(\beta_1 + 4\beta_3)^2}} \qquad (2)$$

Usually, the nonlinear term under the square root can be

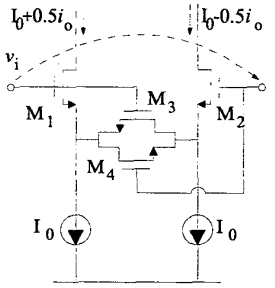

Fig. 2. The MOS transconductor using source degeneration transistors in triode region

made much smaller than unity and improved linearity and larger input dynamic range can be obtained. However, increased linearity means smaller equivalent transconductance and reduced tuning capability. The circuit has bandwidth and noise performances comparable to the simple differential pair.

B. Adaptively biased MOS transconductors

Another topology to achieve high frequency linear MOS transconductors was reported in [2]. The idea is to use a biasing current containing an input dependent quadratic component to cancel the nonlinear term in 1. Thus, if

$$I_0 = I_0' + \frac{\beta {v_i}^2}{8} \qquad (3)$$

the transfer characteristic becomes linear

$$i_o = \sqrt{2\beta I_0'}\, v_i \qquad (4)$$

The required biasing current can be easily obtained using

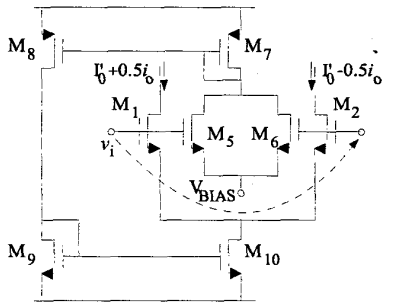

Fig. 3. The adaptively biased MOS transconductor

another two MOS transistors $M_5 - M_6$ having identical transconductance coefficients as the ones in the differential pair $M_1 - M_2$ and two current mirrors $M_7 - M_8$ and $M_9 - M_{10}$ as it is shown on Fig. 3 [3]. The noise generated by the additional squaring circuity does not appear at the output of the transconductor since it is like a common mode voltage at the sources of the differential pair. Due to the effect of the mobility reduction, the size of the transistors in the squaring circuity should be computed as a function of the voltage V_{BIAS} in order to obtain the best linearity. Therefore, tuning the circuit by means of V_{BIAS} will reduce the linearity. The class of input signals which can be processed is limited since the requirement of fully-balanced signals is needed for the squaring circuit to function properly.

C. The novel linear MOS transconductor

We proposed another MOS transconductor that combines the two linearization approaches presented above. Starting from circuit in Fig. 2 and using adaptive biasing current sources, the circuit depicted in Fig. 4 is obtained. To transform the nonlinear transfer characteristic (2) into a linear one, the biasing current I_0 should have the expression

$$I_0 = I_0' + \frac{2\beta_1{\beta_3}^2}{(\beta_1 + 4\beta_3)^2} {v_i}^2 \qquad (5)$$

The transfer characteristic becomes linear and is given by

$$i_o = \frac{4\beta_3\sqrt{2\beta_1 I_0'}}{\beta_1 + 4\beta_3} v_i \tag{6}$$

The adaptive bias current is

$$I_0 = I_{tune} + \frac{\beta_5}{2}\left(\frac{v_i}{2} + V_{GS5} - V_T\right)^2 + \frac{\beta_5}{2}\left(\frac{-v_i}{2} + V_{GS5} - V_T\right)^2$$
$$= I_0' + \frac{\beta_5 {v_i}^2}{4} \tag{7}$$

where

$$I_0' = I_{tune} + \beta_5(V_{GS5} - V_T)^2 \tag{8}$$

Comparing equations (5) and (7), the transconductance coefficient of the squaring circuit is given by

$$\beta_5 = \beta_6 = \frac{8\beta_1{\beta_3}^2}{(\beta_1 + 4\beta_3)^2} \tag{9}$$

Actually, due to the mobility reduction, the sizes of the

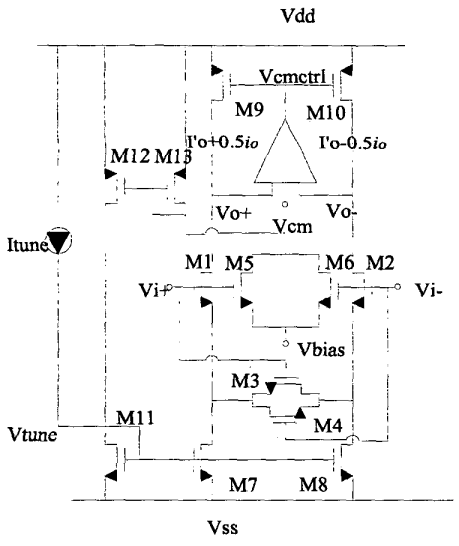

Fig. 4. The novel linear MOS transconductor

transistors M_5 and M_6 are determined empirically. Because β_5 is much smaller than β_1, the dc component of the current generated by the squaring circuity is very small compared to the necessary value required to bias the differential pair. Therefore, the additional current source I_{tune} is needed to tune the transconductor.

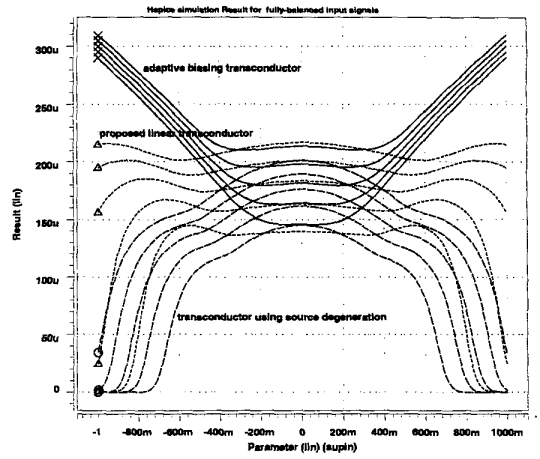

Fig. 5. Spice simulation results for fully-balanced input signals

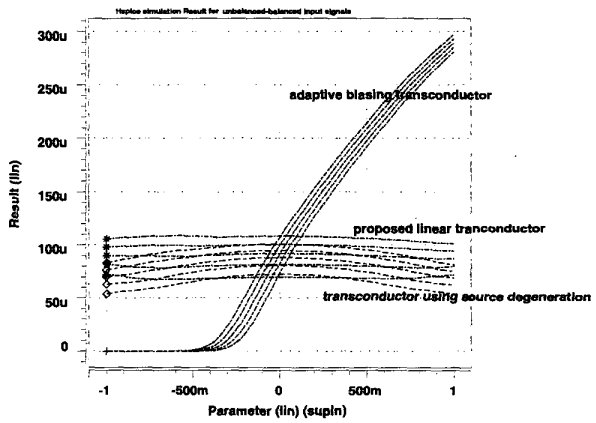

Fig. 6. Spice simulation results for unbalanced input signals

III. Simulation and Experimental Results

The improved linear MOS transconductor has been fabricated using the 0.35μm process from TSMC. The fabricated circuit composites of the novel linear MOS transcouctor, biasing circuit, and commom mode feedback circuitry. The active area is $0.47mm^2$. A single supply voltage of 3.3V is used and the range of the input differential voltage is between -1V to 1V. The simulated transconductance value with fully-balanced input signals is shown in the Fig.5. From the simulation result we can see that the proposed linear MOS transconductor has better linearity than the configurations using only source degeneration and adaptive biasing. For unbalanced input signals (shown in Fig. 6), the linearity of the circuit using only adaptive biasing is destroyed and our circuit is still better than the transconductor using source degeneration.

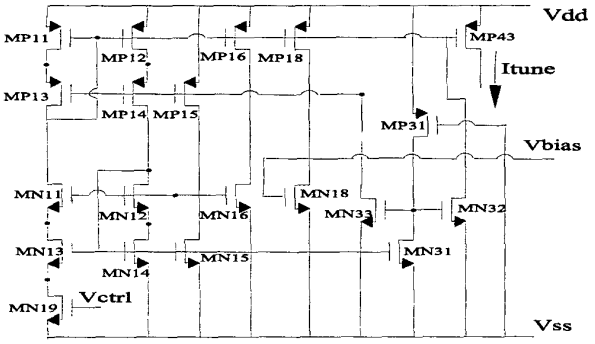

Fig. 7. Circuit diagram of the baising circuitry

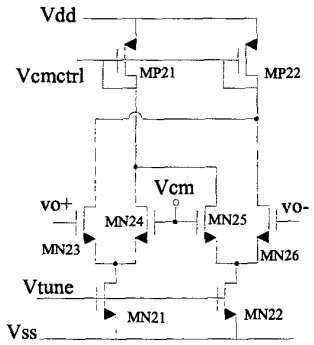

Fig. 8. Circuit diagram of the common mode feedback circuitry

The biasing circuitry which is shown in Fig.7 includes the current mirror and start-up circuit. The current mirror provides wide swing and stable biasing current. The tuning capability of the MOS transconductor is provided by varying the control voltage $Vctrl$, which changes the biasing current. Therefore the transconductor can be tuned as described in the section II.C. The CMFB amplifier is shown in Fig.8. The simulated and measured DC characteristics, and THD are shown in the Fig.9, and Fig10, respectively.

IV. CONCLUSION

The novel linear MOS transconductor, combining the two linearization methods discussed in subsections II.A and II.B and realized in the standard CMOS process, can achieve better linearity compared to the previously reported techniques. It has good tuning capability and range and is functioning for both fully-balanced and unbalanced input signals. The experimental results show good matching with the simulation results in the linearity performance. The circuit can be used in continuous-time filters in which the linearity of transconductor is one of the most critical requirements.

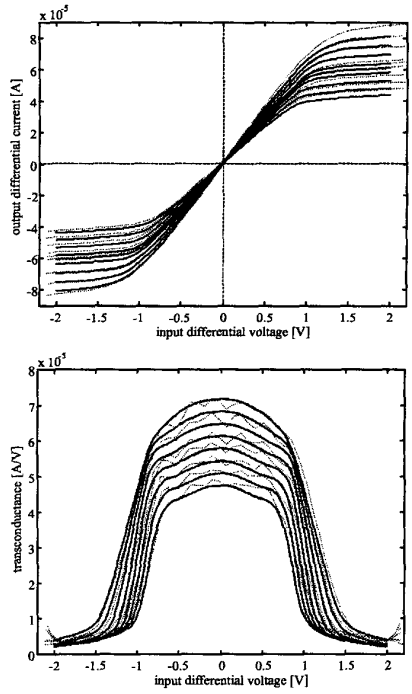

Fig. 9. DC characterics: simulated (dark line) and measured (light line)

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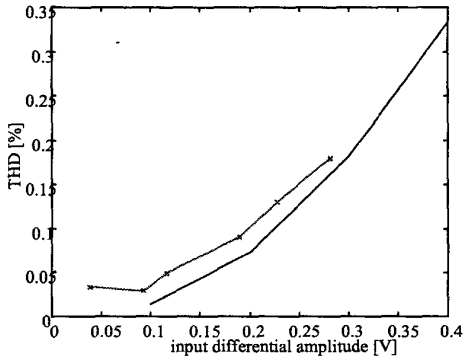

Fig. 10. THD: simulated (dark line) and measured (light line)