

# DESIGN ISSUES FOR LOW VOLTAGE, HIGH SPEED FOLDING AND INTERPOLATING A/D CONVERTERS

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## ABSTRACT

In this paper are discussed design issues for a folding and interpolating A/D converter (ADC) in 0.35  $\mu\text{m}$  CMOS technology. A new averaging technique is used for reducing the DNL and INL errors. The goal is a speed of 100MS/s and a resolution of 10 bits with a supply voltage of 2.5V or less.

## 1. INTRODUCTION

Low latency high-speed A/D converters traditionally employ the flash architecture. The drawbacks of this architecture are the large area required, the large power consumption, the high offset sensitivity, and the large capacitive load at the input. Furthermore, in a low voltage environment the input signal dynamic range will be limited and the precision requirements for the comparators increase. Hence, a 10-bit ADC would require 1024 comparators with less than 0.5mV offset if the input range is 1V.

Folding ADCs utilize nonlinear analog preprocessing of the input signal for reducing the number of comparators. In the classical approach, only one folding signal is used. This signal is quantized to multiple levels. However, the signal nonlinearity (especially at bends) causes significant errors. Next logical step is to use two folding signals offset from each other so that the bent of one corresponds to the zero crossing of the other, and the highly nonlinear part of the signals is never used. Generalizing this method, more folding signals can be generated and quantized to one bit only, dropping completely the linearity requirements (figure 1) [1]. This enables also the extensive use of averaging. Using interpolation for generating additional fine quantization levels from the coarse ones, one can further reduce the amount of hardware and power consumption.

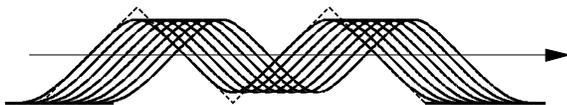


Figure 1. Offset folding signals

Device mismatch creates INL and DNL errors in standard design architecture for flash and folding A/D converters and it is a fundamental drawback in making high-resolution converters. Wider resistors in the reference ladder and larger transistors in the input preamplifiers will improve the precision, but at the cost of increased die size, power dissipation and decreased sample rate. An offset averaging method was firstly introduced in [2] and

consists in the insertion of lateral resistors between the adjacent preamplifier cells of a flash ADC. Offsets are averaged and smaller size devices can be used, resulting in increased operating frequency for the same DNL error. This method has been later extended to folding ADCs.

The main disadvantage of the folding ADC is the reduced bandwidth due to the internal multiplication of the input signal frequency with the folding rate. This problem can be solved employing either a front-end T/H circuit or a distributed T/H circuit after the first folding stage.

In the following section are addressed the trade-offs involved in designing a folding and interpolating ADC using the techniques discussed above. A new method of offset averaging is also presented.

## 2. SYSTEM DESCRIPTION

### 2.1 Overview

A cascaded folding and interpolating topology is used for implementation, interpolation stages being interleaved with folding stages (figure 7). The input signal is sampled by the T/H amplifier and fed to the reference ladders. In the first folding stage, 18 parallel folding signals are generated, each with a folding factor of 5. These signals are interpolated with a factor of two, and folded again with a factor of three. Another interpolation by two is done, and the resulting signals are again folded by three. In the final stage is performed an interpolation by four. For every folding operation in the secondary stages, the number of input signals is decimated by the folding factor, and for every interpolating operation the number of folding signals is multiplied by the interpolating factor. Finally are obtained 32 folding signals with 45 zero-crossings each. Out of the total of 1440 zero-crossings, only the middle 1024 are used for conversion, as the successive averaging distorts the under- and over-flow zero-crossings.

### 2.2 T/H Circuit

As discussed in the first section, a T/H amplifier (THA) is necessary to avoid the cascaded frequency multiplication in folding circuits which leads to severe bandwidth limitation. Moreover, by keeping the signal constant over a period of time, the necessity of a synchronizing circuit between the coarse and fine bits is eliminated [3].

On the other hand, the THA introduces errors at the input. These errors are amplified in the next stages and can be harmful for a high resolution ADC. An alternative approach is to use distributed sampling after the first stage. In this case, the errors will be divided by the gain of the first stage and averaged. The disadvantage is that the THA should operate at a bandwidth equal to the input signal bandwidth multiplied by the input stage folding factor (in this case 5). In this paper is presented the ADC with the front end THA.

### 2.3 Folding Stages

Three folding stages are cascaded to obtain the final folding rate of 45 that cannot be achieved in only one stage. The gate-to-source effective voltage of a differential pair is  $V_{GSeff} = \frac{DR}{2 * N}$ , where DR is the dynamic range of the input signal and N is the folding rate. For a dynamic range of  $1.6V_{pp}$  and a folding rate of 45, in a first order approximation,  $V_{GSeff}$  is less than 20mV. Such a low gate-to-source voltage implies increased noise and a slow device.

The folding rate is distributed over three stages with individual folding rates of 5, 3 and 3. Thus, for the first stage,  $V_{GSeff}$  is increased to 160mV.

Choosing an overall folding rate and distributing it among folding stages is subject of a number of compromises. Having a high folding rate in the early stages will decrease the amount of hardware required. But the folding amplifiers with higher folding rate have longer settling time, and higher sampling rates can be obtained if the highest folding rate is assigned to the final stage, as the errors given by incomplete settling are less harmful.

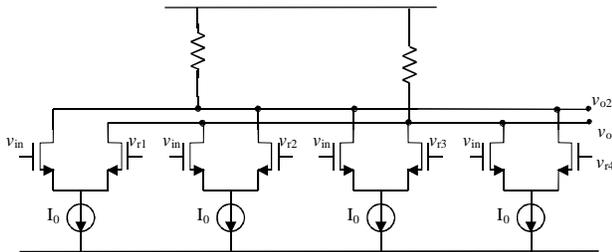


Figure 2. MOS folding amplifier

The number of zero-crossings in the first stage can be written as the product between the folding rate and the number of folding stages:  $Z=MXN$ . Choosing the number of the output folding signals ( $M$ ) large the complexity of the subsequent hardware is increased and the advantage over the flash architecture diminishes. Choosing a large folding rate ( $N$ ),  $V_{GSeff}$  of the differential pairs is decreased with the disadvantages exposed before. Also the number of the folding signals available for averaging is decreased and the effectiveness of the offset averaging operation decreases.

In the subsequent folding stages, either folding by alternate sign summation or folding by analog multiplication can be chosen. The first method is based on the fact that adding offset folding signals with alternate sign, the obtained signal has a higher folding degree. This approach relies on the high harmonic

content of the signal, rectangular input folding signals being optimal. Because the spatial filter used for averaging removes the higher order harmonics of the folding signals, which become almost sinusoidal, additional amplifiers should be introduced between the first and the second, respectively the second and the third, folding stages. Only odd folding rates can be conveniently implemented with this method.

On the other side, the multiplication used in the second method is a nonlinear operation and there is no need for additional amplifiers. The amplitude of the output signals does not depend on the harmonic content. In CMOS, the implementation of a multiplier is neither very facile nor compact, compared to the bipolar case. However, a folded Gilbert cell can be used because we are interested in zero-crossings of the signal, and not in an accurate multiplication. The CMOS Gilbert cell rather performs the operation  $A\sqrt{B}$  than  $AB$ , but the zero crossings are preserved. This method can be used for implementing both odd and even folding rates.

Alternate sign summation is chosen for the implementation of the ADC presented, mainly due to its compactness. The structure of the secondary folding circuits is the same as in first stage (figure 2) [4]. The only difference is that no reference voltages are needed, offset differential folding signals from the previous stage being applied at the inputs. The differential pairs provide the additional gain needed and the alternate sign summation is done in the output nodes.

### 2.4 Offset Averaging

The accuracy of the folding amplifier shown in figure 2 is affected by transistor and resistor mismatches. Offset averaging is employed to improve the accuracy of the converter without increasing the transistor sizes. All folding stages use second order active averaging for the reasons discussed in the following.

As shown in [5], offset averaging can be seen as spatial filtering. For the general structure of a linear spatial filter shown in the figure 3, the following equations can be written [6]:

$$y[n] = b(y[n-2] + y[n+2]) + a(y[n-1] + y[n+1]) + (1-2a-2b)x[n]$$

$$a = \frac{R0}{R1 // R2 + 2R0} \frac{R2}{R1 + R2}$$

$$b = \frac{R0}{R1 // R2 + 2R0} \frac{R1}{R1 + R2}$$

The current sources  $I[n]$  represent the inputs whereas the node voltages  $y[n]$  are the outputs. The resistor indexes show how many nodes the corresponding resistor spans. The second order averaging network depicted here can be generalized to higher orders, but second order will suffice for our application. Equation (1) describes a fourth order non-causal IIR filter with a frequency response given by:

$$H(\omega) = \frac{1-2a-2b}{1-2a\cos\omega-2b\cos2\omega}$$

The random offsets introduced by the mismatch of the transistors forming the differential pairs, the tail currents mismatch and by the limited precision of the reference ladder can be seen as

additive white noise, and the averaging network acts as a low-pass spatial filter, removing the out of band noise. Nevertheless, the number of folding amplifiers limits the improvement achievable by using this method.

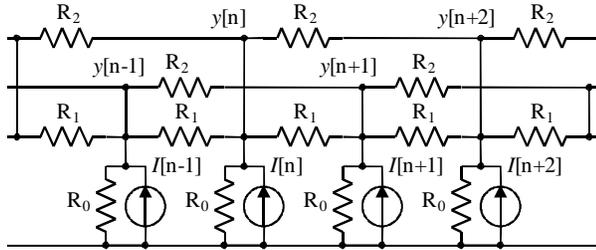


Figure 3. Resistive spatial filter

In the case of a first order averaging network ( $R2 \rightarrow \infty \Leftrightarrow b=0$ ), the implementation is reduced to inserting lateral resistors between adjacent folding amplifiers. The bandwidth of the filter is a function of the  $R1/R0$  ratio and tends to zero as  $R1/R0 \rightarrow 0$ . However, this will affect also the signal, and the effective INL and DNL improvement is actually worsened.

For a second order averaging network, the optimum low pass filter is shown to be obtained for  $b=-a/4$  [6]. Such a filter will have a higher attenuation in the stop-band and a flatter frequency response in the pass-band, therefore the errors will be more efficient removed compared to the first order passive averaging network. In terms of circuit elements, the negative coefficient requires a negative resistor that is implemented with a negative impedance converter (NIC – Fig. 5). The bandwidth of the resulting active filter is set by the  $R1/R0$  ratio. Part of the resulting folding stage is depicted in Fig. 4.

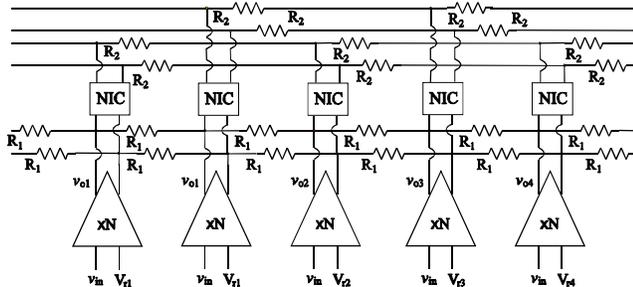


Figure 4. Active resistive offset averaging

Active averaging allows the decrease of the transistor area, hence decreasing the parasitic capacitances and increasing the speed. The NIC transistors can be minimum size because their matching is not important and the additional resistive grids can be minimum-width. Also, compared to passive averaging, it does not decrease the gain of the folding amplifier as the roll-off slope of the spatial filter is steeper and less useful signal is eliminated. This translates at the circuit level in a larger impedance seen by the amplifier, a part of the current taken by the first order positive resistors being compensated by the second order negative resistors.

Aside from efficient offset averaging, another advantage brought by the use of NICs results from the fact that a capacitor connected at the second port of the NIC will appear as negative capacitor at the output of the folding amplifier. The parasitic

capacitance at the output node of the folding amplifier can be therefore compensated with MOS capacitors and the settling time significantly decreased (or, equivalently, the bandwidth is increased). The folding amplifier with NIC and compensating capacitors requires much less power and area than an equivalent folding amplifier having the same settling time.

Figure 6 shows the improvement in DNL and INL for the ADC due to the averaging. In the input stage the DNL is decreased 20 times and the INL 2.3 times, without sacrificing the gain.

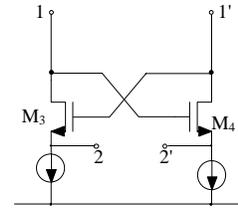


Figure 5. MOS differential negative impedance converter (NIC)

## 2.5 Interpolating Stages

In order to generate additional zero-crossings either current or voltage (resistive) interpolation can be used. Current interpolation is based on the summation of currents reflected through current mirrors with different ratios [7]. It proves to be power hungry and not very precise due to the non-idealities of the current mirrors.

For these reasons, resistive interpolation is preferred. In the first two stages, the interpolation factor is two and in the last stage is four. As described in [8], interpolation by two will generate the correct zero-crossings, but the straightforward approach used here for the interpolation by four will introduce errors. However, these errors are introduced in the last stage and they prove to be negligible.

Due to the averaging performed in every folding stage, the interpolation comes naturally. The lateral resistors are already implemented for averaging and the interpolating signals are obtained from taps in the resistive strip.

## 3. CONCLUSIONS

In this communication a design procedure for a CMOS implementation of a 10 bits, 100MS/s folding and interpolating ADC is presented. A high folding rate is achieved employing cascaded folding. The extensive use of offset averaging in all folding stages increases the speed and accuracy. Additional fine quantization levels are generated in three interpolation stages leading to area and power savings. Future work will be aimed towards expanding the resolution of the ADC without decreasing the speed.

## 4. REFERENCES

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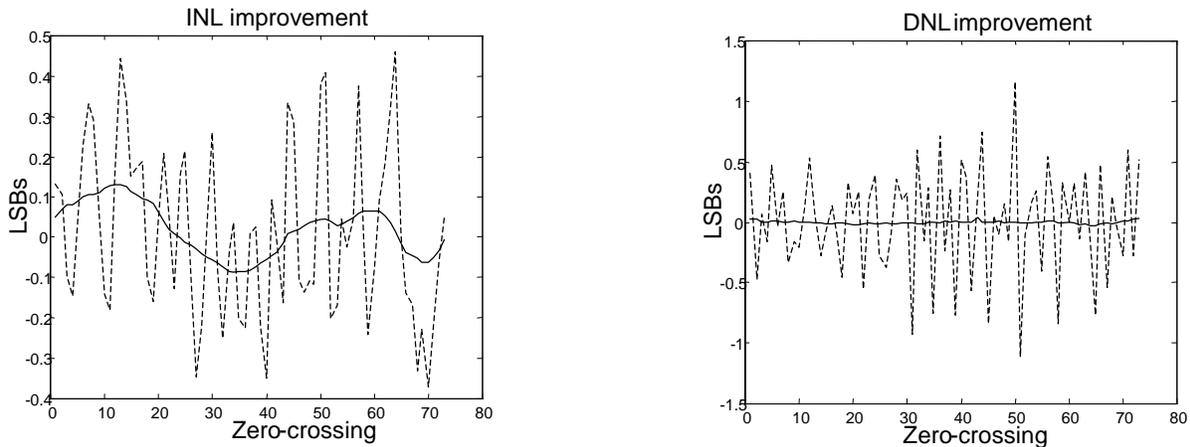


Figure 6. INL and DNL before (dashed line) and after offset averaging

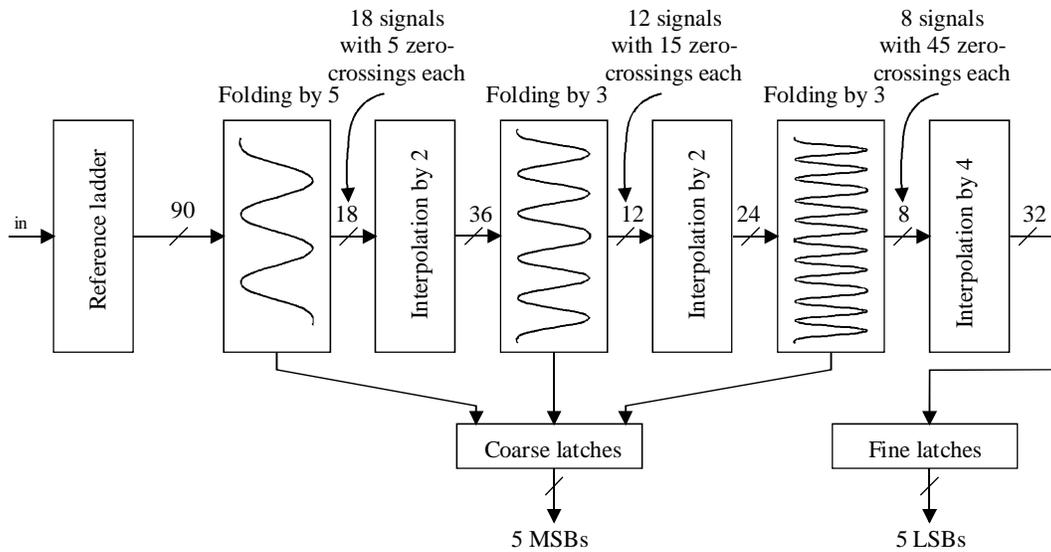


Figure 7. Folding and interpolating ADC