A 1.8V CONTINUOUS-TIME DELTA-SIGMA MODULATOR WITH 2.5MHZ BANDWIDTH

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ABSTRACT

This paper describes the implementation of a low-voltage, wide bandwidth, continuous-time low-pass $\Delta\Sigma$ modulator. The presented modulator operates at a supply voltage of 1.8V and can achieve a maximum SNDR of 74dB (more than 12 bits) for an oversampling ratio of 32 and in a bandwidth of 2.5 MHz

1. INTRODUCTION

Delta-Sigma($\Delta\Sigma$) modulation is a popular technique for performing high-resolution analog-to-digital conversion of relatively low-bandwidth signals [1]. These oversampled data converters avoid many of the difficulties encountered with conventional Nyquist-rate converters, such as requiring precise analog components and abrupt cutoffs in the analog anti-aliasing filter. The noise-shaping loop filter of a $\Delta\Sigma$ modulator can be implemented as a discrete-time system (switched-capacitor, switched op-amp) [2] or as a continuous-time one (active-RC or transconductor-C) [3]. The majority of $\Delta\Sigma$ modulators reported in literature are implemented using switched-capacitor circuits mainly because these realizations are compatible with standard CMOS processes, are insensitive to clock jitter, and the frequency response of the noise shaping filter can be precisely set by capacitor ratios.

Nowadays there is increasing interest in continuous-time implementations of $\Delta\Sigma$ modulators, especially for high-speed and low-power applications. This is primarily due to some important advantages continuous-time realizations have compared to their switched-capacitor counterparts: can operate at higher sampling frequencies, the errors of the sample-and-hold circuit are suppressed by the loop filter, provide implicit anti-alias filtering, and are less prone to pick-up digital noise. Most of the reported continuous-time implementations are band-pass ones and some of these are not using CMOS technology, but silicon bipolar or other processes. There are only few reported CMOS realizations of low-pass continuous-time $\Delta\Sigma$ modulators, either for low-frequency applications [3], or having modest SNR values, below 60dB. The performance of continuous-time $\Delta\Sigma$ modulators is limited by several factors: the nonlinearity of the integrating stages, the thermal and 1/f noise of MOS transistors, the errors introduced by the feedback DAC (loop delay, memory effect, clock jitter). The next section addresses all these critical design issues for continuous-time $\Delta\Sigma$ modulators and presents solutions to eliminate them or at least, to diminish their effect. Section 3 introduces the circuit implementations of the modulator's building blocks: transconductor, comparator, feedback DAC, and in section 4 behavioral simulations results are shown. Finally, some conclusions and future research directions are given.

2. SYSTEM-LEVEL DESIGN ISSUES

Due to the sampling operation inherently present in a $\Delta\Sigma$ modulator, independent on how the loop filter is implemented (switched-capacitor or continuous-time), such a system is a discrete-time one. Therefore, the design of a CT $\Delta\Sigma$ modulator starts from a discrete-time prototype satisfying the desired performance (SNR, BW, OSR) and using discrete-time to continuous-time transformations to obtain the parameters of the CT realization [4], [5]. To meet our proposed target (SNR $>$72dB, BW=2.5MHz, OSR=32), a fourth-order, inverse Chebyshev, noise transfer function has been chosen, the topology of the modulator beeing shown in Fig. 1.

2.1. Nonlinearity of the integrating stages

One of the most critical aspects in continuous-time $\Delta\Sigma$ modulators design is the nonlinearity of the integrating stages. For high-speed applications a transconductor-C ($G_m - C$) approach is used for implementing the loop filter. To characterize the effect of nonlinearity of integrating stages on the achievable SNDR, we assumed a cubic type nonlinearity for the $i - v$ transfer characteristic of the transconductors: $i = G_m\left(v - nv^3\right)$. Behavioral simulations have been carried out for the proposed modulator shown in Fig. 1, considering the effect of the nonlinearity in each stage separately. Fig. 2 depicts the drop in SNDR as a function of the nonlinearity coefficient n. The simulation results show that the first two integrating stages must have very good linearity and nonlinearity of last stage has a negligible effect on SNDR.

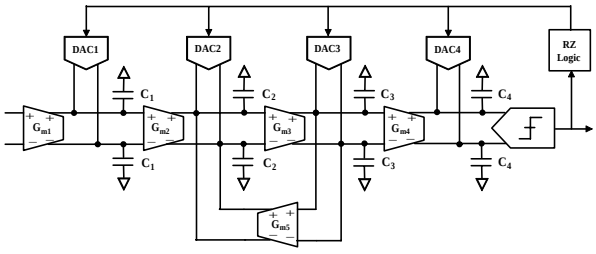

Figure 1: Block diagram of the $\Delta\Sigma$ modulator.

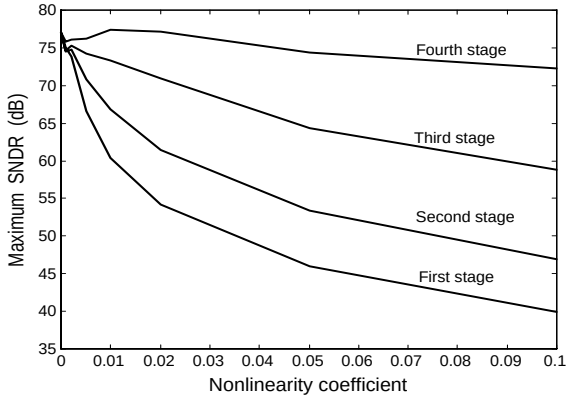

Figure 2: The effect of nonlinearity of integrating stages.

2.2. Finite gain of op-amps/OTAs

The performance of a $\Delta\Sigma$ modulator may also be degraded by the integrator leakage resulting from the finite dc gain of op-amps or OTAs. The limited gain moves the NTF zeros away from their ideal positions, which reduces the amount of attenuation of the quantization noise in the baseband, and consequently a the drop in the SNR results. Since the leakage of the integrators is inversely related to the dc gain, the gain must be increased to the point that the overall modulator performance is not degraded. The result in [6] demonstrates that if the dc gain of integrators is equal or larger than the oversampling ratio, the SNR drops less than 1dB.

2.3. Noise

In a CMOS $\Delta\Sigma$ modulator, circuit noise comes from two main sources: thermal noise and 1/f noise. The noise of the first integrating stage is dominant and will determine the performance of the entire $\Delta\Sigma$ modulator. The input referred thermal noise is inversely proportional to the transconductance G_m of the OTA, so larger G_m is required for reducing the thermal noise contribution. Larger G_m can also make bandwidth larger. The price paid for this is power consumption increase. Flicker (1/f) noise is extremely important in low-pass CMOS $\Delta\Sigma$ modulators, because it dominates at low frequencies, where low-frequency noise increases with 10dB/dec with decreasing frequency. In SC implementations one uses correlated double sampling techniques to reduce the amount of 1/f noise, but this approach should be avoided in CT implementations to preserve their advantages. Because1/f noise is inversely proportional to the area of MOS transistors, one can increase their size to decrease 1/f noise, but this will increase the capacitance of MOS transistors and the bandwidth decreases. One should make reasonable tradeoff among noise, bandwidth and power consumption for the requirements of the entire $\Delta\Sigma$ modulator. Because the first integrating stage is the most critical one from the noise point of view, the feedback topology shown in Fig. 1 has been chosen. This topology requires lower unit gain frequency for the first integrating stage, therefore one can uses larger transistors to minimize 1/f noise. Large transconductance and large capacitors are used in the first integrating stage to decrease the thermal noise contribution.

2.4. Memory effect and loop delay of the feedback DAC

Continuous-time $\Delta\Sigma$ modulators are known to suffer from asymmetric pulses or memory effect of the feedback DAC [7], which is caused by the unequal rise and fall times of the DAC output current pulses. This effect leads to a decrease of the dynamic range and introduces even harmonic distortion. For a given samping rate, OSR, and desired SNR, the maximum pulse asymmetry (τ) must approximately satisfy the relation [5]

$$\tau \leq \frac{4 \cdot T_s \cdot \sqrt{OSR}}{SNR_{desired}}. \quad (1)$$

Two solutions to the memory effect have been proposed. The first one is to use a current steered differential pair to implement the fully differential feedback DAC. It is demonstrated in [8] that the sum of two asymmetric differential DAC waveforms produces a symmetric DAC waveform. The second solution is to use return-to-zero DAC pulses although this will increase the number of transitions in the DAC current.

In a practical CT $\Delta\Sigma$ modulator, there exists loop delay between the quantizer clock and DAC current pulse due to the nonzero switching time of the transistors in the feedback path. Loop delay is detrimental to the performance of higher-order modulators. The maximum input stable amplitude will decrease with increasing loop delay. The performance loss due to loop delay can be greatly mitigated using return-to-zero DAC pulses.

3. CIRCUIT IMPLEMENTATION

The proposed fourth-order low-pass continuous-time $\Delta\Sigma$ modulator with inverse Chebyshev type noise transfer function is shown in Fig. 1, and consists of four cascaded $G_m -$

C integrators and a local resonator feedback to realize the desired finite transmission zero. A topology with distributed feedback has been chosen because of its lower complexity and minimum power dissipation compared to all other possible configuration achieving the same SNR for the same oversampling ratio.

3.1. Linear CMOS transconductor

As mentioned before, the linearity of the integrating stages is critical to the overall performance of the final modulator. Especially for high resolution A/D converters, the first integrating stage needs highly linear transconductors to satisfy the required SNDR. Because MOSFET-only transconductors have linearity of only 40-60dB, a novel highly linear resistor-based transconductor has been developed [9] for the proposed $\Delta\Sigma$ modulator. The circuit implementation of the transconductor is shown in Fig. 3. It consists of a main MOS differential pair M_1-M_2 with resistive source degeneration and an additional pair of op-amps to increase the linearity. The two op-amps are implemented using two single transistor stages: M_7, M_8 with active loads M_9-M_{10}. The inverting stages $M_{11} - M_5$, $M_{12} - M_6$ are used to achieve negative feedback. Because moderate gain op-amps are required to obtain the required linearity, the load for the second stage of the op-amps, M_5-M_6, are connected as diodes to achieve stability without compensation. The tranconductance is equal to 1/R. The transconductor has been designed and simulated using a CMOS 0.25 μm process. The Hspice simulation results show that the achieved THD is better than -80dB up to 2.5 MHz for a 0.8 V_{p-p} input differential voltage at a single 1.8V supply voltage. The total input referred equivalent noise voltage is around 30 μV_{rms} in a bandwidth from dc to 2.5 MHz for R=3 kΩ.

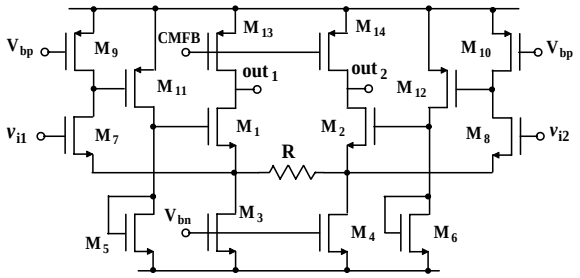

Figure 3: Resistor-based highly linear transconductor.

3.2. Comparator

In single-bit $\Delta\Sigma$ modulators the performance of the comparator is not critical. Because the comparator is inside the feedback loop, the errors introduced by its offset and hysteresis and any additional sampling errors are noise shaped (similarly to quantization noise) by the loop filter. Therefore the requirements of the comparator are relaxed. Fig. 4 shows the schematic of the comparator used in the proposed modulator [10].

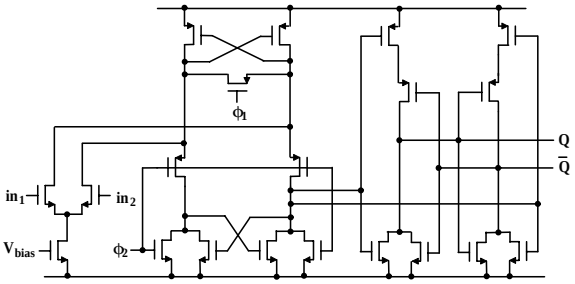

Figure 4: Schematic of the CMOS comparator.

3.3. Feedback DAC

Because the feedback DAC is connected to the output of the integrators, the switching moments of the current-steering transistors depend on the instantaneous output voltage. This introduces additional nonlinear distortions. To minimize this effect, a modified, cascode type current-steering feedback DAC in Fig. 5 has been used in the proposed modulator. MOS capacitors M_{d1}, M_{d2}, M_{d3}, M_{d4} controlled by Q_{RZ2} and Q_{RZ1} respectively, are used to compensate the errors due to charging and discharging active transistors M_{s1}-M_{s2} and M_{s3}.

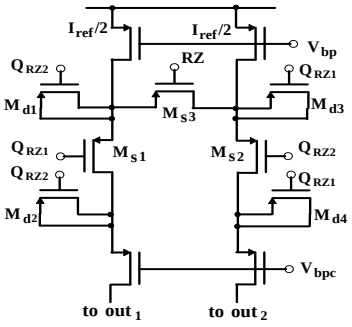

Figure 5: Cascode current-steering feedback DAC.

4. SIMULATION RESULTS

The loop filter coefficients of the modulator in Fig. 1 are scaled to maximize the overload level of the entire modulator by using all of the available signal swing at the output of each integrator without clipping. The modulator parameters after scaling are shown in Table 1. A behavioral model for the $G_m - C$ integrating stages, taking into account their

nonlinearity and leakage, and the finite bandwidth of the transconductor, has been developed (Fig. 6). The modulator has been simulated in Matlab's Simulink. The behavioral simulation results are shown in Fig. 7. The ideal modulator can achieve a maximum SNR of 76 dB. With a dc gain of 100 for each integrator and the nonlinearity coefficients of integrating stages of 0.1%, 0.2%, 0.2% and 1%, respectively, including the loop delay of 20% of the clock cycle, the SNDR is decreased by 4 dB. By using return-to-zero DAC pulses, the modulator can obtain the maximum SNDR of 74.

Table 1: Modulator parameters (G_{m5}=32 μS)

$Stage$	1	2	3	4
$G_m(\mu S)$	560	280	186	93
$C(pF)$	40	8.9	3.8	1.1
$I_{DAC}(\mu A)$	355	128	79	33

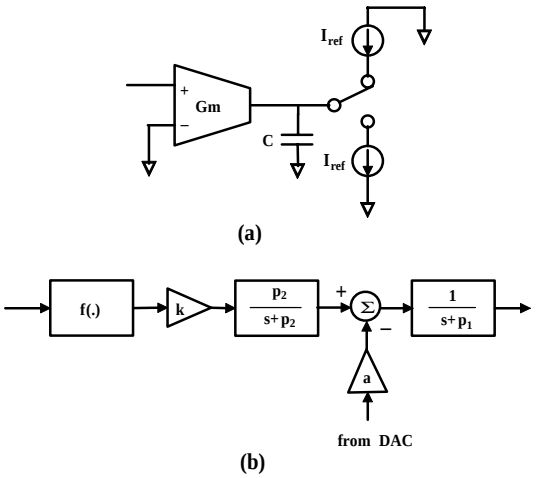

Figure 6: Behavioral model (b) of the $G_m - C$ integrator (a)

5. CONCLUSIONS

A low-voltage, wide bandwidth, fourth-order continuous-time low-pass $\Delta\Sigma$ modulator is presented. The critical aspects in the design of the continuous-time $\Delta\Sigma$ modulators have been investigated and solutions to them have been proposed. The behavioral simulation results have demonstrated that the proposed modulator can achieve the maximum SNDR of 74 dB in a bandwidth of 2.5 MHz for an oversampling ratio of 32. The layout of the proposed modulator is currently under development and transistor-level simulations have to be carried out to verify the behavioral simulation results.

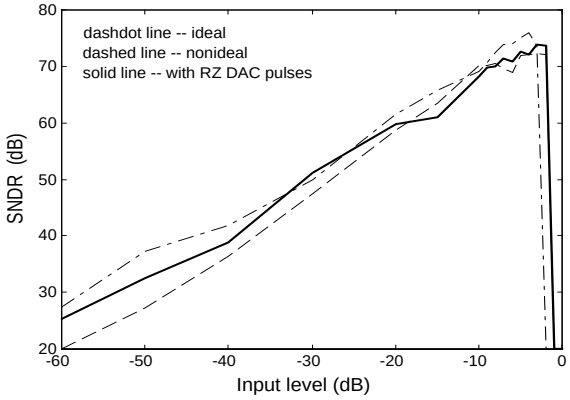

Figure 7: SNDR vs input level.

6. REFERENCES

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