A CONTINUOUS-TIME $\Delta\Sigma$ MODULATOR WITH 63-DB DYNAMIC RANGE AND 500KHZ BANDWIDTH IN $0.35\mu m$ SOI CMOS TECHNOLOGY

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***Abstract*— This paper describes the implementation of a continuous-time low-pass $\Delta\Sigma$ modulator in SOI CMOS technology. Modulator operates at a supply voltage of 3.3V, uses an oversampling ratio of 32 and can achieve a maximum dynamic range of 63dB (more than 10 bits) in a bandwidth of 500KHz.**

I. INTRODUCTION

Delta-Sigma ($\Delta\Sigma$) oversampling A/D converters (ADC) can achieve high resolutions with relatively simple circuit complexity and by using low precision analog components [1], being nowadays the preferred approach for low and medium frequency applications. The noise-shaping loop filter of a $\Delta\Sigma$ modulator (the core of the $\Delta\Sigma$ ADC) can be implemented either by using discrete-time circuitry (switched-capacitor, switched op-amp) or continuous-time one. Most of the reported realizations use the switched-capacitor approach because the coefficients of the noise-shaping filter can be precisely set by capacitor ratios and high resolutions can be achieved. However, continuous-time $\Delta\Sigma$ modulators can operate at higher sampling frequencies, consume less power, provide implicit anti-alias filtering, and the sampling errors are suppressed by the loop filter. Whereas in the past continuous-time $\Delta\Sigma$ modulators have been implemented in bipolar processes, currently more and more CMOS implementations are reported in literature [2], [3].

Silicon on insulator (SOI) CMOS technology can achieve higher operation speed and lower power dissipation than traditional bulk CMOS processes [4], [5]. SOI CMOS differs from bulk CMOS by placing a silicon oxide insulator layer between the top active silicon and the bottom silicon substrate, which minimizes the capacitance of the gate area. In SOI technology, the transistors are isolated from one another with trench-type isolation which is not susceptible to electrical latchup and is significantly more area efficient than junction isolation. The oxide isolation successfully inhibits the noise caused by crosstalk, capacitive coupling and switching, especially the noise coupling through the wafer substrate. Another advantage of SOI CMOS is its radiation hardness compared to bulk CMOS, which makes it desirable in space and military applications. With these distinct features, SOI is expected to break into the main IC industry and truly provide mixed signal designers with innovation opportunities to implement SoC (system-on-a-chip) applications.

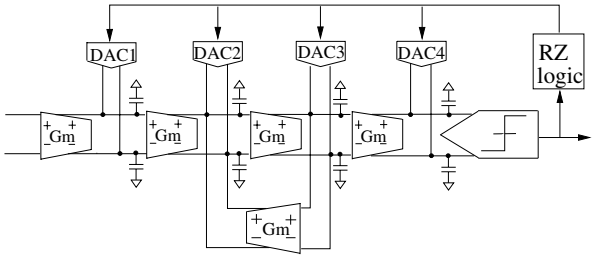

Fig. 1. Block diagram of the $\Delta\Sigma$ modulator

With its benefits being investigated in digital circuits for some years, the exploitation of SOI CMOS for analog and mixed signal circuit design has lagged behind bulk CMOS, but is receiving more and more interest in last few years. Up to our knowledge, there are only few implementations of switched-capacitor $\Delta\Sigma$ modulators in SOI CMOS, but no continuous-time ones. In this communication a continuous-time implementation of a 4th-order $\Delta\Sigma$ modulator using Honeywell's 0.35 μm partially depleted SOI CMOS process is presented. The next section reviews the critical design issues of continuous-time $\Delta\Sigma$ modulators. Section 3 presents the prototype chip and its experimental characterization, and finally, section 4 concludes the paper.

II. DESIGN ISSUES

Due to the sampling operation inherently present in a $\Delta\Sigma$ modulator, independent on how the loop filter is implemented (switched-capacitor or continuous-time), such a system is a

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discrete-time one. Therefore, the design of a continuous-time (CT) $\Delta\Sigma$ modulator starts from a discrete-time prototype satisfying the desired performance: signal-to-noise ratio (SNR) and bandwidth. By using discrete-time to continuous-time transformations the parameters of the CT realization [6], [7] are derived. For the presented system a fourth-order, modified inverse Chebyshev noise transfer function has been chosen. The topology of the modulator is shown in Fig.1. The loop filter consists of four cascaded integrators and a local resonator feedback to realize a finite transmission zero. The distributed feedback topology has been selected because of its lower power dissipation compared to other possible configurations achieving the same SNR for a given oversampling ratio. For high-speed applications, the transconductor-C ($G_m - C$) is the preferred approach to implement the integrators because it presents high input impedance and achieves low power consumption.

A. Noise and circuit non-idealities

In a CMOS realization circuit noise comes from two main sources: thermal noise and $1/f$ noise. The noise of the first integrating stage is dominant and will determine the performance of the entire $\Delta\Sigma$ modulator. Because the thermal noise is inversely proportional to the transconductance G_m of the operational transconductance amplifier (OTA), large transconductance values and large capacitors are used in the first integrating stage to decrease its thermal noise contribution. The price paid for this is an increase in the power consumption. Flicker $(1/f)$ noise is extremely important in low-pass CMOS $\Delta\Sigma$ modulators, because it dominates at low frequencies, where low-frequency noise increases with 10dB/dec with decreasing frequency. Because $1/f$ noise is inversely proportional to the area of MOS transistors, large area devices are used in the input differential pair of first stage OTA. However, as pointed out before, due to the silicon oxide insulator, enlarging the size of SOI MOS transistor will not cause significant capacitance increase and bandwidth loss as in the case of bulk CMOS. Moreover, because the distributed feedback topology shown in Fig.1 requires a low unit gain frequency for the first integrating stage, the power consumption is minimized even when large area devices are used.

The integrator nonlinearity has a critical influence on the performance of continuous-time $\Delta\Sigma$ modulators. To quantify-how linear each integrating stage should be for a given signal to noise and distortion ratio (SNDR), behavioral simulations have been carried out in Matlab's Simulink by using a cubic nonlinearity to model the $i - v$ transfer characteristic of the MOS transconductor: $i = G_m(v - nv^3)$. Fig.2 depicts the drop in SNDR as a function of the nonlinearity coefficient n. The simulation results show that the first two integrating stages must have very good linearity, whereas the nonlinearity of the last stage has a negligible effect on SNDR.

The integrator leakage resulting from the finite DC gain of opamps or OTAs is another non-ideality degrading the performance of the $\Delta\Sigma$ modulator. The limited DC gain moves

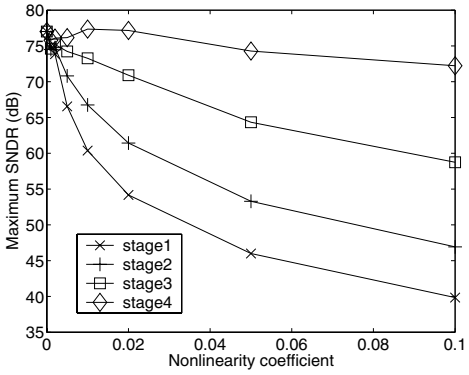

Fig. 2. Effect of integrator nonlinearity on SNDR

the zeros of the noise transfer function (NTF) away from their ideal positions, which reduces the amount of attenuation of the quantization noise in the baseband, and consequently generates a drop in the SNR. Therefore, the gain should have a large enough value, so that the overall modulator performance is not degraded. The result in [8] demonstrates that if the DC gain of integrators is equal to or larger than the oversampling ratio, the SNR drops less than 1dB.

Continuous-time $\Delta\Sigma$ modulators are known to suffer from asymmetric pulses or memory effect of the feedback DAC [9], which is caused by the unequal rise and fall times of the DAC output signal. This effect leads to a decrease in the dynamic range and introduces even harmonic distortion. To eliminate the memory effect, two approaches have been combined in the design of the feedback DAC. First, a current steering differential pair implements a fully differential feedback DAC. It is demonstrated in [10] that two asymmetric single-ended DAC waveforms produce a symmetric differential DAC waveform. The second approach is to use a return-to-zero (RZ) DAC pulse shape. The RZ DAC pulses are also used to mitigate the performance loss caused by loop delay between the quantizer clock and DAC output due to the nonzero switching time of the transistors in the feedback path.

B. Circuit implementation

As pointed out at the beginning of this section, the loop filter integrators use a transconductor-C implementation. The schematic of the transconductor [11] is shown in Fig.3. Basically, it consists of a MOS differential pair with resistive source degeneration (M_1, M_2, R) and an additional pair of op-amps to increase its linearity. The op-amps are implemented as simple differential pairs ($M_{11} - M_{12}$ respectively $M_{21} - M_{22}$) with current mirrors as loads. Two level shifters ($M_3 - M_5$ respectively $M_4 - M_6$) ensure a low voltage operation. Cascode tail current sources are used for achieving good CMRR, whereas the cascode active loads ($M_{31} - M_{34}$) guarantee a large DC gain. The small-signal transconductance is approximately equal to $1/R$. Hspice simulation results show that the achieved total harmonic distortion (THD) is lower than -80dB up to 2MHz for a 0.8 V_{p-p} differential input voltage.

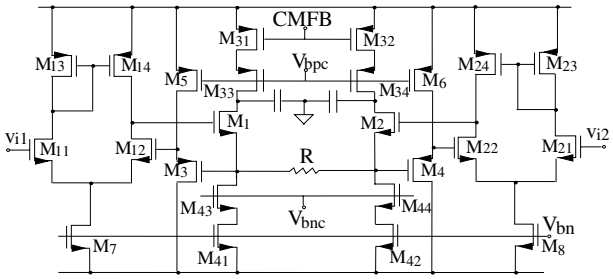

Fig. 3. Resistor-based highly linear transconductor

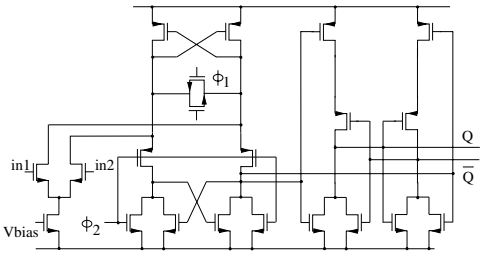

Fig. 4. Schematic of the CMOS comparator

The total input referred equivalent noise voltage is around 20 μV_{rms} in a bandwidth from DC to 500KHz for R=18kΩ.

The high-speed latched comparator [12] shown in Fig.4, is used as an one-bit internal ADC. For single-bit $\Delta\Sigma$ modulators the performance of the comparator is not critical. Because the comparator is inside the feedback loop, the errors introduced by its offset and hysteresis, and any additional sampling errors are shaped (similar to quantization noise) by the loop filter. Therefore the requirements of the comparator are relaxed.

Fig.5 shows the schematic of the current steering fully differential feedback DAC used in the modulator. To eliminate the effect of the loop delay between the sampling clock and the DAC output, a RZ logic block is used to control the feedback DAC. Because the feedback DAC is connected to the output of the integrators, the switching moments of the current steering transistors depend on the instantaneous output voltage. This introduces additional nonlinear distortions. To minimize this effect, a cascode current source has been used in the DAC.

III. EXPERIMENTAL RESULTS

The continuous-time $\Delta\Sigma$ modulator has been fabricated using a 0.35μm Partially Depleted SOI CMOS process from

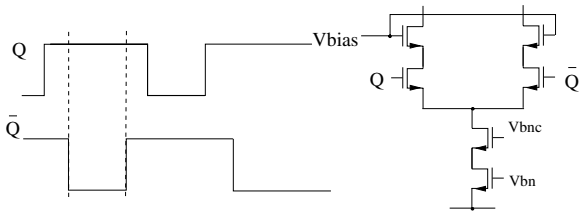

Fig. 5. Current-steering feedback DAC

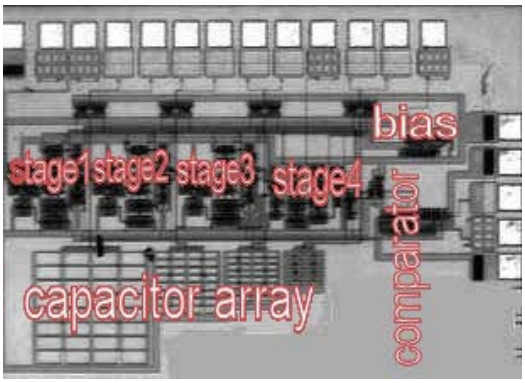

Fig. 6. Photograph of the fabricated modulator

Honeywell. In partially depleted SOI (PD-SOI) CMOS the depletion regions do not reach through the entire silicon channel/body region. By comparison, in the less complex manufactured fully depleted SOI (FD-SOI) process, the channel region is fully depleted. On the other hand, PD-SOI MOS transistors, compared to their fully depleted counterparts, have reduced parasitic source-drain depletion capacitances. The internal substrate of PD-SOI MOS transistors (the body) is floating. Its potential depends on the different charges injected into or extracted from the body region, which can cause some design issues different from bulk CMOS, like kink effect and history effects. In the case of Honeywell's SOI CMOS process, a body-to-source tie is used to stabilize threshold voltage and floating body related effects.

The fabricated chip microphotograph is shown in Fig.6. The modulator occupies an area of $1.8 \times 0.9mm^2$ (excluding the pads and monitoring amplifiers). Thanks to the structure advantage and excellent noise immunity provided by SOI, the layout can be more compact because the devices are isolated from each other. At the same time, no guard ring is needed, which is indispensable in the bulk CMOS case. Due to the relatively large (18$\sim$80 kΩ) source degeneration resistors of the OTAs, p-well resistors are used. Although the accuracy and the linearity of p-well resistors is not so good as that of polysilicon resistors, they still can satisfy the requirements for a 10-bit ADC.

The test setup uses a 32MHz crystal oscillator to supply the sampling clock to the modulator. The differential input signal is supplied by an Agilent 33250A waveform generator and coupled through a high-frequency transformer. The digital output data stream of the modulator was captured using a HP 1660A logic analyzer and the post-processing was performed using MATLAB. The spectrum of the output signal is computed using a 8192-point Hanning windowed FFT. Fig. 7 shows the spectrum of the output signal in the case of a single-tone test ($F_{in} = 125KHz, V_{in} = -3$ dBFS). For comparison, the spectra in ideal case (obtained by running Matlab behavioral simulations) and for the complete circuit simulated in Hspice are also shown in the same plot. Fig. 8 shows the resulting SNR and SNDR versus the normalized input signal,

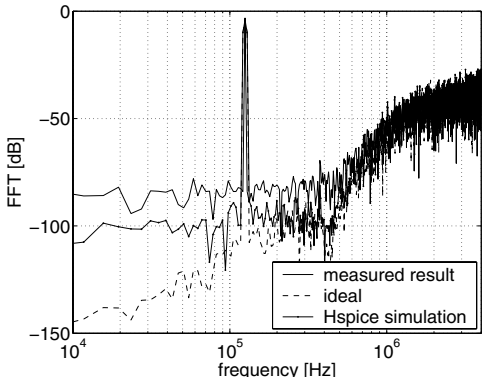

Fig. 7. Simulated and measured spectra of the modulator

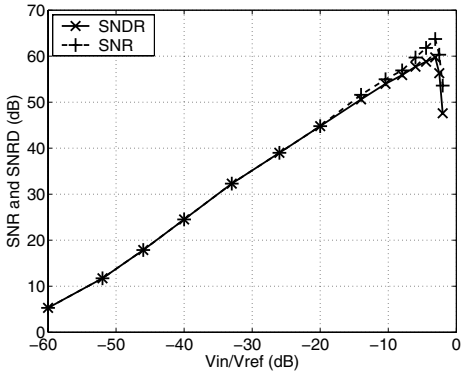

Fig. 8. Measured SNR and SNDR vs input level

for a single-tone test using a 125-KHz input frequency. Up to -3 dBFS input, the quantization noise energy is dominant over the level of the harmonics. For larger input amplitudes, the internal ADC goes into overload and distortions increase. From Fig. 8, the input amplitude for which SNR=0dB can be extrapolated to -66dB.

The fabricated continuous-time modulator achieves 63-dB dynamic range (resolution $>$ 10 bits), 63.73-dB SNR, and 59.84-dB SNDR over 500KHz signal bandwidth with an oversampling ratio of 32, while dissipating 12mW from a 3.3V supply. The experimental results are summarized in TABLE I.

TABLE I
PERFORMANCE SUMMARY

Specification	Value
Signal bandwidth	500KHz
Sampling frequency	32MHz
Oversampling ratio	32
Dynamic range	63 dB
SNR	63.73 dB
SNDR	59.84 dB
Supply voltage	3.3 V
Power consumption	12 mW
Technology	0.35μm SOI CMOS
Silicon area	$1.8 \times 0.9mm^2$

IV. Conclusion

The technology advantages of the SOI CMOS technology make it an ideal process to implement high quality, low power and area efficient mixed signal ICs. A continuous-time $\Delta\Sigma$ modulator with 63- dB dynamic range over 500KHz input signal bandwidth has been implemented using a $0.35\mu m$ SOI CMOS process from Honeywell. The lack of expertise in the design of SOI CMOS analog and mixed signal circuits and the need for obtaining a first-run operational prototype required conservative specifications to be imposed on this design. In the near future a multi-bit, continuous-time $\Delta\Sigma$ modulator using the same SOI CMOS technology will be designed and fabricated. The anticipated performance of the future modulator is a bandwidth of $2.5 \sim 5$ MHz, resolution $>$ 12 bits and low power dissipation. The fabricated modulator has also to be tested for radiation hardness, these results to be published elsewhere.

Acknowledgment

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