Single Event Transients Characterization in SOI CMOS Comparators

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***Abstract*—A theoretical analysis of single event induced transients in SOI CMOS comparators is presented, confirmed by transistor-level simulations. The proposed approach can predict the probability of single event upset (SEU) at the output of the comparator. A design methodology to achieve an imposed radiation hardness is proposed.**

***Index Terms*—Comparators, single-event effects, SOI CMOS circuits.**

I. Introduction

AMONG all radiation effects in electronic circuits, probably the most difficult to characterize are single event effects (SEEs). Depending on the type of the circuit hit (digital or analog) and on the energy of the striking particle, one can have different effects induced by single radiation events [1]: single event upset (SEU) [2], single event latchup (SEL), single event transient (SET) [3], or even single event gate rupture (SEGR) [4]. While in the case of digital circuits there are well defined measures to quantify the single event effects, there is no equivalent standardized methodology in the case of analog circuits. The single exception to this statement are the comparators which are basic building blocks in analog-to-digital converters (ADCs) and realize the interface between the analog circuitry and subsequent digital processing systems. Therefore, one can characterize the SEEs in comparators by using SEU, a measure that is characteristic of digital circuits.

Most of the reported research results describing SETs in analog circuits have been based on experimental techniques [2]–[5]: either by directly irradiating the circuits by using heavy-ion beams, or by exciting the devices with laser pulses. Extremely few articles present analytical studies of single event events on analog circuits and supply circuit design techniques to mitigate these effects [6]. In this paper, we present an analytical method to characterize SETs in SOI CMOS comparators with the proposed ultimate goal of being able to predict the probability of upset at the output, given the parameters of the circuit, hit location and energy, and amplitude of the input voltage. The choice for SOI CMOS technology for this study is motivated by several reasons: 1) it is one of the options for the future in the International Technology Roadmap for Semiconductors (ITRS), based on the anticipated economic benefit (lower power dissipation, lower supply voltage, reduced stray capacitances, therefore higher bandwidth) [7], [8]; 2) it inherently presents some radiation hardness; and 3) the SEEs are easier to characterize because the effects are localized to a single device.

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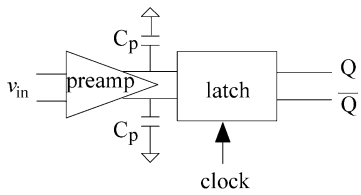

Fig. 1. Simplified structure of a latched comparator.

The outline of this communication is as follows. In Section II, the general structure of a latched comparator is presented and its operation, both in a radiation-free environment and when affected by single radiation events, is described. A simplified linear model for the comparator is introduced and the concept of SEU critical time is proposed. Section III reviews a previously reported SEE model for the SOI MOSFET and the comparator chosen as a test benchmark for SEE is described. Comparative simulation results, using the behavioral model for the comparator and the transistor-level circuit, are presented. Finally, Section IV concludes with some circuit design techniques to mitigate the SEE in comparators.

II. SEE Model for a Latched Comparator

For high-speed operation, the configuration of a CMOS comparator is usually chosen to keep its complexity to a minimum. For most of the reported implementations, the comparators can be equivalently reduced to the basic diagram shown in Fig. 1. The input preamplifier acts as a buffer between the driving circuitry and the latch, minimizing the kickback effect. The latch loads the preamplifier and presents either a positive input resistance (during the reset or regeneration phase), or a negative resistance (during the latch phase). The capacitors C_p are the stray capacitances at the output of the amplifier. It is important to note that, to achieve high-speed operation and to minimize the memory effect of the comparator (hysteresis), the absolute value of the latch input resistance should be as small as possible, both during the regeneration and latch phases.

Modeling the preamplifier as a voltage controlled current source driven by the input voltage $v_{\rm in}$, the equivalent single-ended circuit of the latched comparator is shown in Fig. 2(a). $R_{\rm latch}$ is the equivalent input resistance of the latch, having a positive value R^+ in the reset phase, respectively a negative value $-R^-$ in the latch phase. The output voltage is clipped to

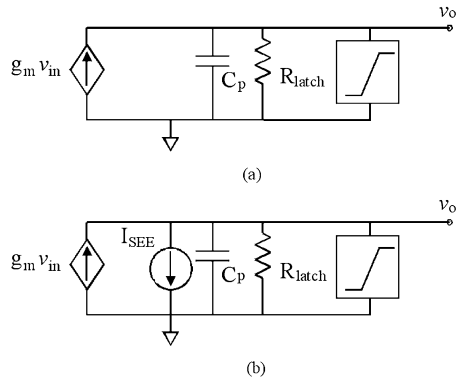

Fig. 2. Equivalent single-ended model for a latched comparator: (a) radiation-free environment; (b) affected by SEE.

some saturation voltages $\pm V_{\rm sat}$, this effect being modeled by the limiting circuitry shown in Fig. 2(a). The operation of the comparator comprises two phases: the reset (or regeneration, or track) phase and the latch (or comparison) phase. In the following, it is assumed that the input voltage does not change within a clock cycle. During the reset phase, the output voltage decreases exponentially (with the time constant $\tau^+ = C_p R^+$) from either $+V_{\rm sat}$ or $-V_{\rm sat}$ to the steady state value set by the input voltage and the gain of the preamplifier, $A_v = g_m R^+$, according to

$$v_o(t) = \pm V_{\rm sat} e^{-t/\tau^+} + g_m v_{\rm in} R^+ (1 - e^{-t/\tau^+}). \qquad (1)$$

Let T_1 be the duration of the regeneration phase. At the end of the regeneration phase the output voltage is $V_{\rm reg} = v_o(T_1)$ and if T_1 is large enough, the steady state is reached $V_{\rm reg} \approx v_o(\infty) = g_m v_{\rm in} R^+$. This value represents the unbalance voltage at the input of the latch that will decide its output logic level. During the comparison phase, the latch presents a negative input resistance and the voltage v_o increases exponentially (with the time constant $\tau^- = C_p R^-$) from the value $V_{\rm reg}$ to, theoretically, infinity:

$$v_o(t) = V_{\rm reg} e^{t/\tau^-} - g_m v_{\rm in} R^- (1 - e^{t/\tau^-}). \qquad (2)$$

Although during the latch phase the output voltage is also slightly influenced by the input voltage, its effect is negligible. The polarity of the voltage $V_{\rm reg}$ established at the end of the reset phase will decide if one goes toward plus or minus infinity. As shown in Fig. 2, a limiting circuitry is nonetheless present in the comparator model and eventually the output voltage will be clipped to the saturation voltages (approximately equal to the supply voltages) and the latch supplies at its output the logic levels "0" or "1."

When a certain transistor in the comparator is hit by an ionizing particle, electron–hole pairs are generated in the substrate. In the case of SOI CMOS technology, the generated charges cannot migrate to other devices, as in the case of bulk CMOS technology. Therefore, the entire process is localized within a single device. Depending on MOSFET's operation mode, part of the ionization charge will be drawn by the drain terminal, generating a photocurrent (which can also be amplified by the parasitic bipolar transistor). Eventually, depending on the topology of the circuit and the hit location, a smaller or larger current pulse $I_{\rm SEE}$ is injected into the output of preamplifier and the equivalent model shown in Fig. 2(b) is valid. One has to remark that one cannot approximate the single effect induced current

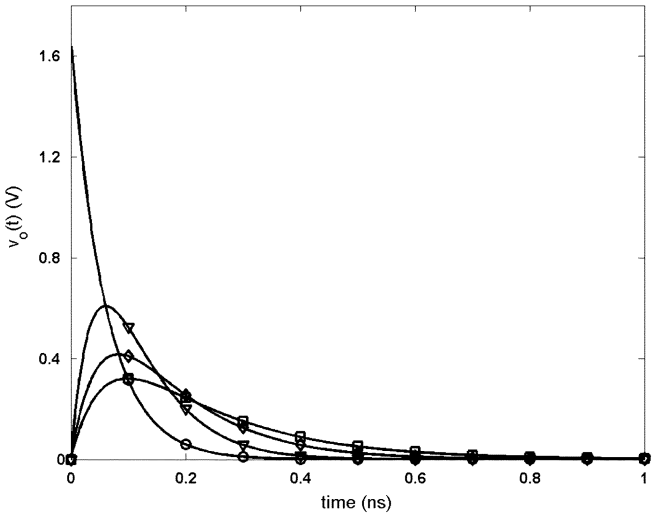

Fig. 3. Voltage transient in (4): $\circ - \tau = 0; \triangledown - \tau = 60$ ps; $\diamond - \tau = 120$ ps; $\square - \tau = 180$ ps.

waveform by a Dirac impulse because the output node is characterized by a small time constant (both R^+ and R^- have low values). The following simplifying assumptions are used for the analysis of SEE in the comparator: 1) the SEE current has a waveform described by a decreasing exponential

$$I_{\rm SEE}(t) = I_0 e^{-t/\tau} \qquad (3)$$

carrying the charge $Q_{\rm SEE}$, where $Q_{\rm SEE} = \int_0^\infty I_{\rm SEE}(t)\,dt = I_0\tau$; 2) the input voltage of the comparator does not change during a clock cycle (quasi-static operation or a sample-and-hold circuit is present at the input); and 3) the SEE induced transients are small enough to maintain a linear operation of the comparator during the regeneration phase and during the latch phase (at least until clipping occurs). There are two possible cases: the hit occurs during the reset phase, or the hit occurs during the latch phase. As it will be shown in the following, the most critical hit corresponds to the regeneration-to-latch transition.

If the SEE hit occurs during the regeneration phase, the preamplifier output voltage will contain, besides the terms in (1), an additional SEE component given by

$$v_{\rm SEE}(t) = -\frac{R^+ I_o \tau}{\tau - \tau^+} \left(e^{-(t-t_{\rm hit})/\tau} - e^{-(t-t_{\rm hit})/\tau^+} \right) \sigma(t - t_{\rm hit}) \qquad (4)$$

where $\sigma(t)$ is the Heaviside step function and the hit is supposed to occur $t_{\rm hit}$ seconds after the beginning of the regeneration phase. The amplitude and duration of such a transient will be a function of hit energy ($Q_{\rm SEE} = I_0\tau$), the time constant associated to the SEE current pulse τ, and circuit parameters (R^+, τ^+). For the correct operation of the comparator, the SEE induced transient must decay within $(T_2 - t_{\rm hit})$ seconds below the steady-state value of the output voltage in the radiation-free environment, $V_{\rm reg} = g_m R^+ v_{\rm in}$. Fig. 3 depicts the waveform described by (4) for $Q_{\rm SEE} = 0.1$ pC, $R^+ = 1\,\text{k}\Omega, \tau^+ = 60$ ps, and different values of τ. One can see that a Dirac impulse $(\tau = 0)$ modeling the SEE current pulse generates the largest amplitude, but the shortest duration (set by the circuit time constant). Although at the first sight this case may be seen as the most advantageous one because the SET decays very quickly after the

hit, a large amplitude transient changes the operating mode of the MOSFETs and the circuit is not linear anymore, as it was assumed at the beginning of our analysis. Therefore, the transient may last longer than predicted by (4) because some devices may have to resume their default operating mode.

If the hit occurs during the latch mode, an additional transient component contributes to the ideal output voltage in (2):

$$v_{\rm SEE}(t) = \frac{R^- I_o \tau}{\tau + \tau^-} \left(e^{-(t-t_{\rm hit})/\tau} - e^{(t-t_{\rm hit})/\tau^-} \right) \sigma(t - t_{\rm hit}). \tag{5}$$

The decision of the comparator will be set by the sign of the final output voltage, that is by the sum of the two dominant terms in $v_o(t)$, one dependent on $V_{\rm reg}$, the other one induced by the single event hit.

It is clear now, from the way the SEE affects the comparator, that the closer the hit to the regeneration-to-latch transition, the worse is its effect because 1) in the regeneration phase the circuit has less time to recover from the hit, and 2) in the latch phase the ideal output voltage has not increased yet to sufficiently large amplitudes and the single-event hit may change its polarity. Let us define a measure called critical time and defined as the time window around the regeneration-to-latch transition moment within which a SEE hit of a certain energy generates upset. The total critical time is the sum between the critical time in the regeneration phase $t_{\rm cr1}$ and the critical time in the latch phase $t_{\rm cr2}$. The critical time in the regeneration phase is the solution of the equation

$$g_m R^+ v_{\rm in} - \frac{R^+ I_o \tau}{\tau - \tau^+} (e^{-t_{\rm cr1}/\tau} - e^{-t_{\rm cr1}/\tau^+}) = 0 \tag{6}$$

which does not have a closed analytical solution but in a single case, $\tau = 0$. This corresponds to modeling the SEE current pulse by a Dirac impulse carrying the finite charge $Q_{\rm SEE} = I_0 \tau$. Thus, replacing $I_0 \tau$ by $Q_{\rm SEE}$ in (6) and making $\tau = 0$, one has

$$t_{\rm cr1} = \tau^+ \ln \left(\frac{Q_{\rm SEE}}{g_m \tau^+ v_{\rm in}} \right) \tag{7}$$

where $\tau^+ = R^+ C_p$. The critical time in the latch phase is the solution of

$$V_{\rm reg} e^{t_{\rm cr2}/\tau^-} - \frac{R^- I_0 \tau}{\tau + \tau^-} = 0 \tag{8}$$

where from

$$t_{\rm cr2} = \tau^- \ln \left[\frac{R^- Q_{\rm SEE}}{g_m R^+ (\tau + \tau^-) v_{\rm in}} \right]. \tag{9}$$

If we assume $\tau \ll \tau^-$, the critical time in the latch phase is

$$t_{\rm cr2} = \tau^- \ln \left[\frac{Q_{\rm SEE}}{g_m \tau^+ v_{\rm in}} \right]. \tag{10}$$

Therefore, by modeling the SEE current waveform by a Dirac impulse, the total critical time $t_{\rm cr}$ becomes

$$t_{\rm cr} = t_{\rm cr1} + t_{\rm cr2} = (\tau^+ + \tau^-) \ln \left(\frac{Q_{\rm SEE}}{g_m \tau^+ v_{\rm in}} \right). \tag{11}$$

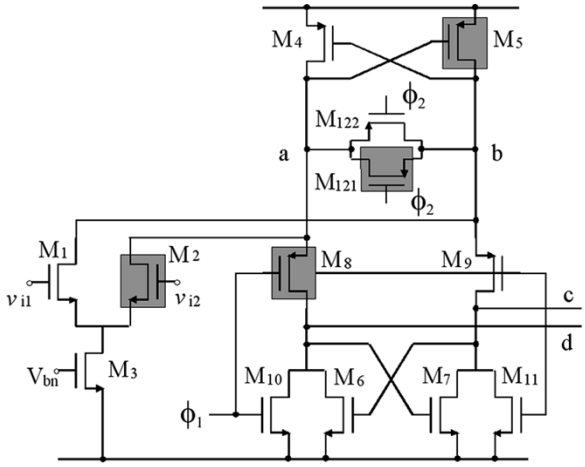

Fig. 4. Schematic of the simulated comparator.

The larger the comparator time constants, the larger the critical time will be. This implies that the probability of the bit error will also be larger. Assuming that the amplitude of the current pulse which simulates the effect of the radiation has a normal distribution, the charge $Q_{\rm SEE}$ will also be characterized by a normal distribution with mean μ_Q and standard deviation σ_Q. A simple calculus shows that the distribution function of the critical time is

$$F(t_{\rm cr}) = P(t_{\rm cr} \le t) = \Phi \left[\frac{v_{\rm in} g_m \tau^+ \exp\left(\frac{t}{\tau^+ + \tau^-}\right)}{\sigma_Q} - \frac{\mu_Q}{\sigma_Q} \right] \tag{12}$$

where Φ is the cumulative distribution function of the normal distribution. If we assume that N is the number of particles per (second*mm ^{2}) and the area of the tested device is $A_{\rm device}$, then the bit error rate (BER) can be expressed as number of particles hitting a transistor with area $A_{\rm device}$ during $t_{\rm cr}$($N\, A_{\rm device} t_{\rm cr}$). The distribution function of the bit error is

$$P(e \le e_x) = \Phi \left[\frac{v_{\rm in} g_m \tau^+ \exp\left[\frac{e_x}{(\tau^+ + \tau^-) N\, A_{\rm device}}\right]}{\sigma_Q} - \frac{\mu_Q}{\sigma_Q} \right] \tag{13}$$

where e_x is an imposed bit error rate (BER) value.

III. Simulation Results

In order to verify the correctness of the theoretical analysis presented in Section II, we chose the practical CMOS comparator [9] shown in Fig. 4, transferred the design into a partially depleted SOI CMOS process available from Honeywell and performed a comprehensive set of transistor-level HSpice simulations. The comparator is controlled by two nonoverlapping clock signals ϕ_1 and ϕ_2. During the regeneration phase, ϕ_1 is high and ϕ_2 is low. The small signal resistance loading the preamplifier implemented by the differential pair $M_1 - M_2$ is

$$R^+ = \frac{1}{4 g_{o12} - g_{m4}}$$

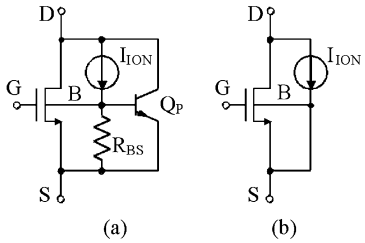

Fig. 5. (a) SOI MOSFET SEE model in [10] and (b) simplified model.

where g_{o12} is the drain-to-source conductance of either M_{121} or M_{122}, and g_{m4} is the transconductance of $M_4 - M_5$. The comparator switches to the latch phase by first making ϕ_2 high and, after some delay, ϕ_1 low. When ϕ_2 goes high, the first analog latch $(M_4 - M_5)$ is enabled and the differential voltage v_{ab} is increased quickly by its positive feedback, the resistance in the latch phase being given by

$$R^{-} = \frac{1}{g_{o4} - g_{m4}}.$$

The second analog latch $(M_6 - M_7)$ is enabled after a short time and the comparator output voltage is delivered between nodes (c) and (d). The equivalent voltage to v_o in the model shown in Fig. 2, is v_{ab}, the output of the preamplifier. Therefore, the single-effect event critical devices are the ones emphasized in Fig. 4.

The study of the single event effects has been achieved by using the single event effect model for SOI MOSFETs introduced in [10]–[12] and depicted in Fig. 5(a). In this model, it is considered that the source is tied to the body (as in the case of Honeywell's SOI CMOS process), the resistor $R_{\rm BS}$ modeling the finite resistance between the hit point and the body-to-source tie location. The current source $I_{\rm ION}$ represents the photocurrent generated by the ionizing particle and Q_p is the parasitic bipolar transistor of the SOI MOSFET. Because our simulations are intended to supply less quantitative and more qualitative results (as accurate model parameter values for $R_{\rm BS}$ and Q_p are not available) and since the only effect of the parasitic bipolar transistor is to increase the amplitude of the current $I_{\rm ION}$, we have used in our simulations the simplified model shown in Fig. 5(b). As in [10], the ionization current pulse is represented by a double exponential with time constants of $\tau_1 = 10$ ps and $\tau_2 = 200$ ps associated to the rise and fall times, respectively. However, compared to the original paper introducing this SEE model where these values were not critical because the time constants of the simulated circuits were much larger than the duration of the pulse, in the case of a high-speed comparator the SEE current pulse shape is critical. Nevertheless, not having more accurate SEE model data available, we have adopted in our simulations the same values as in [10]. The total charge carried by the current pulse is $Q_{\rm ION} = I_{\rm ION}(\tau_2 - \tau_1)$ where $I_{\rm ION}$ is the amplitude of the two exponentials. One has to remark that $Q_{\rm ION}$ is not equal to $Q_{\rm SEE}$ in the equations in Section II. $Q_{\rm SEE}$ is the charge carried by the equivalent current source connected to the output node of the preamplifier, whereas $Q_{\rm ION}$ is the charge generated within a hit device, and $Q_{\rm SEE} = KQ_{\rm ION}$, where K represents a charge gain (that can be even smaller than unity) which is dependent on the circuit topology and parameters. However, for the considered comparator this gain is approximately equal to unity for the transistors M_2, M_5, and M_8, whereas the gain is twice as large for M_{121} and M_{122} because equal charges are delivered at both drain and source terminals and the change in the differential voltage v_{ab} is double.

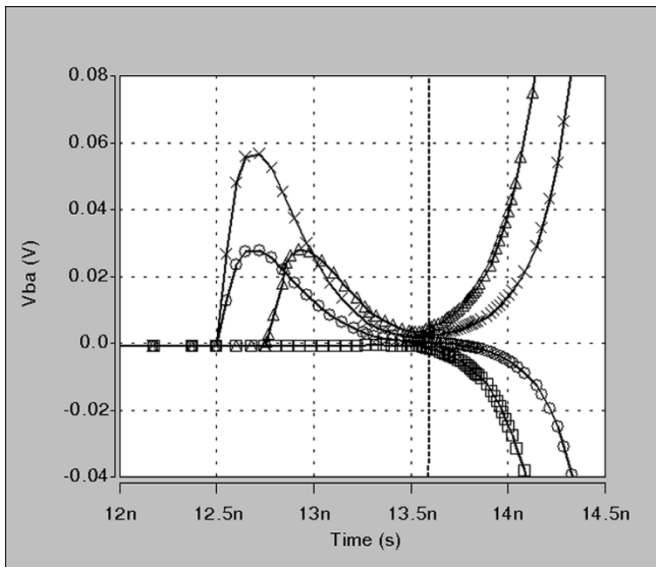

Fig. 6. Transients in the regeneration phase: □—no SEE hit; △—small amplitude hit occurring within its critical time; ∘—small amplitude hit occurring beyond its critical time; ×—large amplitude hit occurring within its critical time.

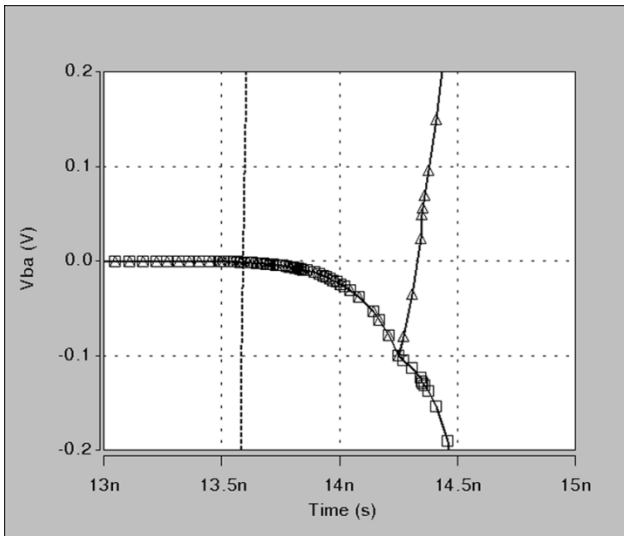

Fig. 7. Transients in the latch phase: □—no SEE hit; △—SEE hit occurring within its critical time.

In our approach, all transistors (actually, only half of them because the circuit diagram is perfectly symmetric) have been sequentially augmented with the current source $I_{\rm ION}$. The current pulse occurrence has been adjusted to different time positions within an entire clock cycle, between the beginning of the regeneration phase and the end of the latch phase. The amplitude of the ionization current pulse has been modified to correspond to values of 0.01 pC to 0.1 pC of charge generated in the body of the hit device and the resulting transients have been monitored. The simulation results supplied by HSpice are consistent with the theoretical analysis.

Fig. 6 shows the simulated SETs in the comparator during the regeneration phase, whereas Fig. 7 plots the transients corresponding to a hit during the latch phase. In Fig. 6 several cases are

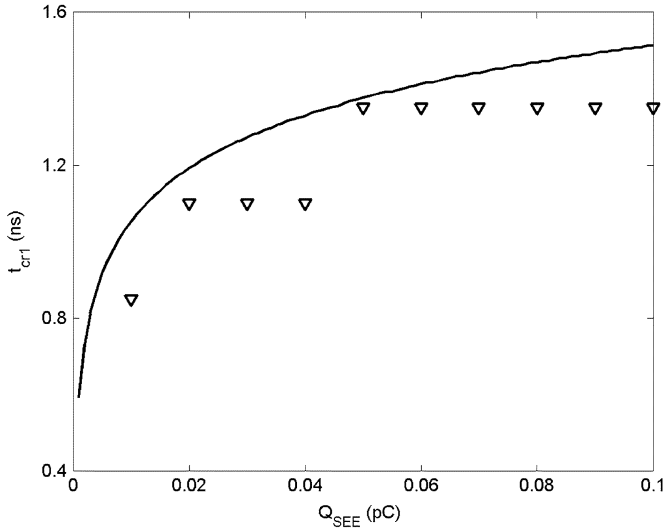

Fig. 8. Simulated (points) and predicted (lines) critical times during the regeneration phase.

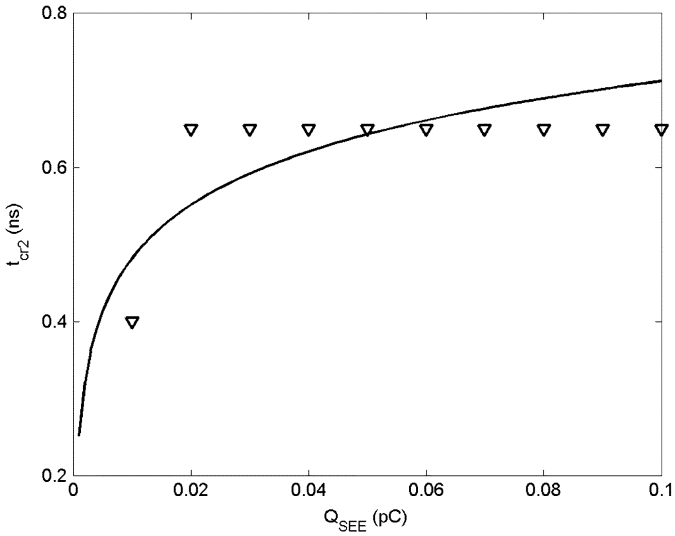

Fig. 9. Simulated (points) and predicted (lines) critical times during the latch phase.

illustrated: the ideal case of no SEE hit when the output voltage goes negative in the latch phase; two hits changing the outcome of the comparator, one smaller and the other one larger, occurring at different moments of time, but both of them within their corresponding critical times; a small hit that does not generate SEU because it occurs beyond its critical time and the circuit has time to recover. We have measured the critical times and compared the results with the ones predicted by (6) and (8) after evaluating the small signal parameters of the simulated circuit. The comparison is depicted in Figs. 8 and 9. In simulations we measured the critical times by using a 0.25-ns time step, this value being a compromise between precision and simulation time. To accurately measure the critical times, the transient simulations should be run by augmenting the SOI MOSFETs with SEE current pulses occuring at moments of time spaced by infinitely small steps and observing for which one of them the comparator is upset. However, the simulation time can increase a lot without supplying any additional significant information since the transistor models used in computing their small signal parameters are very simple. However, considering the 0.25-ns time step used for measuring the critical times from simulations, one can see there is a good agreement between the simulations and the theoretical analysis.

IV. Conclusion

The single event transients in a high-speed SOI CMOS comparator are analyzed. A behavioral SEE model for the comparator is proposed and HSpice simulations have been carried out to verify the validity of the proposed model. The concept of critical time is introduced and evaluated for a given circuit topology and parameters. The critical time can be used to predict the bit error rate by assuming a certain probability distribution function for the energy and rate of single event hits. According to the obtained results, the comparator is quite insensitive to radiation single event effects occurring during the latch phase, but it is very sensitive to even small amplitude pulses that occur around the transition between the reset and latch phases. In order to decrease the probability of the error caused by radiation effect, the comparator should be designed as a high-speed one (with very short regeneration and latch times), but it should be operated at low clock rates because our analysis shows that the SEU probability is directly proportional to the clock frequency and inversely proportional to the speed of comparator.

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