Analysis of Single-Event Effects in Continuous-Time Delta–Sigma Modulators

Adrian Leuciuc, *Member, IEEE*, Bing Zhao, *Student Member, IEEE*, Yi Tian, and Jinhu Sun

***Abstract*—Behavioral simulations are carried out for characterizing single-event effects in continuous-time Delta–Sigma modulators, the core subsystem of an oversampling analog-to-digital converter. The performed study shows that some topologies are less immune than others to single-event hits and that by appropriately choosing the order and oversampling ratio of the modulators one can reduce the radiation effects.**

***Index Terms*—Analog-to-digital data converters (ADCs), Delta–Sigma modulators, single-event effects, silicon-on-insulator complementary metal–oxide–semiconductor (SOI CMOS) circuits.**

I. Introduction

Analog-to-digital data converters (ADCs) are often the bottleneck of every mixed-signal system design. In the context of space applications an ADC must satisfy, besides the requirements for commercial applications, additional ones regarding low power consumption and radiation hardness. Delta–Sigma oversampling ADCs realize an optimum tradeoff between circuit complexity, cost, and power dissipation, high accuracy being achieved with low precision analog components [1]. In this communication we present an analysis of single-event effects (SEE) in Delta–Sigma modulators, the analog core of oversampling ADCs. Although our analysis is confirmed by simulations performed for the particular case of continuous-time implementations of Delta–Sigma modulators, similar results can be derived for switched-capacitor (SC) realizations. Most of the previously reported research results describing SEEs in analog circuits have been based on experimental techniques [2], either by directly irradiating the circuits by using heavy-ion beams or by exciting the devices with laser pulses. The ultimate goal of our work is to develop behavioral SEE models for the basic building blocks in a mixed-signal system (like an oversampling ADC) and to predict its performance by simulations.

The outline of this communication is as follows. In Section II the general structure of an oversampling Delta–Sigma ADC is presented and its subsystems are described. The operation of the analog core of the oversampling ADC, the Delta–Sigma modulator, is explained. Possible effects induced by single-event hits are outlined and behavioral models for the basic building cells are introduced. Section III presents the results of behavioral simulations and in Section IV final conclusions are drawn.

Manuscript received July 20, 2004; revised September 3, 2004. This work was supported by the Air Force Research Laboratory, Space Vehicles Directorate, Kirtland Air Force Base, New Mexico, under Contract F29601-02-2-0299, entitled Mixed-Signal Electronics Technology for Space.

The authors are with the Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, NY 11794 USA.

Digital Object Identifier 10.1109/TNS.2004.839109

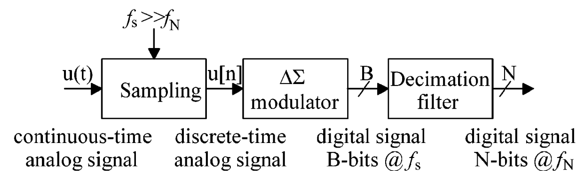

Fig. 1. Structure of an oversampling Delta–Sigma ADC.

II. Delta–Sigma Modulators and Single-Event Effects

The basic structure of an oversampling Delta–Sigma ADC and the type of signals processed by its building blocks are shown in Fig. 1. The input analog signal is sampled with a rate f_s much higher than the Nyquist rate f_N and the samples are processed by the subsequent subsystem, the Delta–Sigma modulator. The modulator contains a low resolution flash ADC that delivers at a very high rate digital words represented on few bits (B). The last block, the decimation filter, down-samples and filters the input signal generating N-bit $(N > B)$ output digital codes at the Nyquist rate, and therefore, oversampling ADC trade resolution in time with resolution in amplitude. Compared to Nyquist-rate ADCs, where one output digital code corresponds to one input analog sample, oversampling data converters do not have a one-to-one correspondence between the input samples and the output digital codes. That is why the performance of an oversampling ADC is not specified by using the classical measures defined for Nyquist-rate ADCs (integral and differential nonlinearity errors), but by dynamic measures imported from communications, such as signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). As it will be pointed out later in the paper, since these measures assume a steady-state operation of the oversampling ADC they cannot be used to characterize the effects of single-event hits. Therefore, a dedicated testing setup had to be developed to study these effects.

The analog core of the oversampling ADCs is the Delta–Sigma modulator, its structure being shown in Fig. 2. The internal ADC is a low-resolution one, usually just a simple comparator. The ADC adds quantization error on its input signal, this error being assumed to be random, uncorrelated with the input signal, and having a flat power spectrum density. The loop filter is designed to leave unchanged the input signal $u[n]$ and to shape the spectrum of the quantization error $e[n]$, thereby removing most of its energy from the band of interest. The loop filter can be implemented either using continuous-time circuitry, or it may have a discrete-time implementation (switched

0018-9499/04$20.00 © 2004 IEEE

Fig. 2. (a) Basic architecture of a Delta–Sigma modulator. (b) Equivalent linear model.

capacitors or switched currents). A digital-to-analog converter (DAC) is present in the feedback path to convert the output digital codes back into the analog domain. The digital low-pass and decimation filter following the Delta–Sigma modulator removes the high-frequency components of the quantization noise, delivering at the output of the overall oversampling ADC a high resolution signal. One has to remark that, although in Fig. 1 a separate sampling block is present at the front-end of the oversampling ADC, in a real implementation the sampling is done either just before the internal ADC in the case of a continuous-time realization, or it is achieved automatically by the inherent operation of the SC/switched-current filter.

In a radiation environment, depending on what subsystem within the Delta–Sigma modulator is affected, one can have different effects. If the loop filter is hit the amplifier gain can change and the frequency response of the loop filter can be modified. Alternatively, the amplifier offsets can change or single-event transients (SET) can occur. In the case the internal ADC is irradiated, the comparators can exhibit larger offsets and/or bit flip-flops are induced (single-event upset, or SEU). The radiation effects on the feedback DAC include increased jitter, nonlinearity errors, and glitches. A block that is not depicted in Fig. 1, but inherently present in the system, is the biasing circuitry. However, most of the time, any radiation-induced errors in the biasing circuitry will behave as common-mode perturbations for the main circuit. Therefore, careful design (e.g., fully differential implementation, high common-mode rejection ratio) can mitigate their effects.

In the following we will restrict ourselves to the study of SEEs in Delta–Sigma modulators and we will consider only continuous-time implementations. This choice is justified by the fact that continuous-time implementations of Delta–Sigma modulators have already proven to offer the advantages of lower power consumption and higher frequency operation compared to their SC counterparts [3], [4]. However, most of our conclusions regarding the system-level design considerations to achieve radiation hardness are valid for SC implementations as well.

Let us now study with more details the internal configuration of the loop filter. Independent of the type of the modulator (low-pass or band-pass), the loop filter consists of a cascade of integrating stages with additional feedback or feed-forward paths, as shown in Fig. 3. For a low-pass modulator some local feedback loops around two integrators may be present or not.

Fig. 3. Topologies for Delta–Sigma modulators: (a) with distributed feedback (FB) and (b) with feed-forward summation (FF).

Fig. 4. (a) Topology and single-event transients in a $G_m - C$ integrating stage of a Delta–Sigma modulator; (b) behavioral model.

Fig. 5. $G_m - C$ integrator using the OTA reported in [5].

An optimized noise transfer function with finite transmission zeros requires the presence of the local feedback paths. In the case of band-pass modulators the local feedback loops are always present, implementing resonators.

The transconductor-C (or $G_m - C$) approach is the preferred one for implementing high frequency continuous-time filters. If the integrator is realized as a $G_m - C$ one, a current-mode feedback DAC can be directly connected at the output of the transconductor, as shown in Fig. 4(a). For high speed operation both the operational transconductance amplifier (OTA) and the DAC require topologies without any high-impedance internal nodes. In this case, an ionizing particle hitting one device within

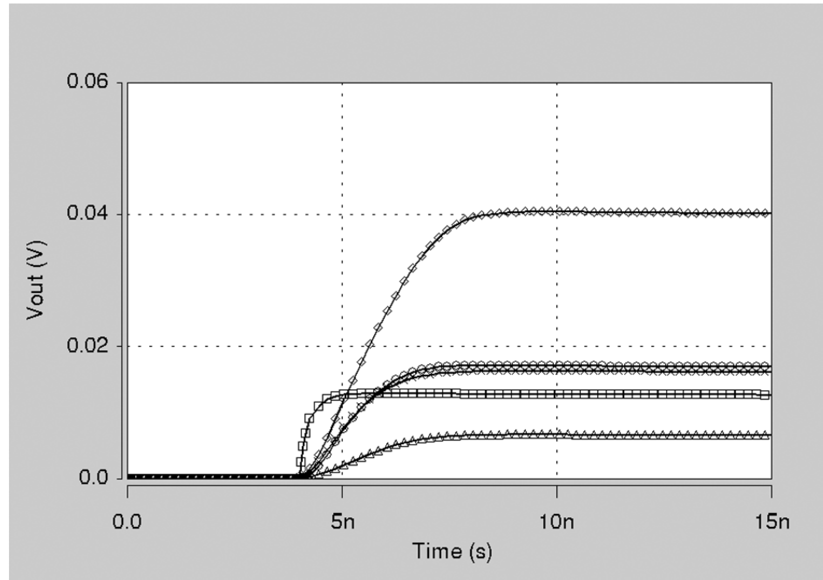

Fig. 6. Simulated SET in the $G_m - C$ integrator in Fig. 5 for $Q_{\rm SEE} = 1$ pC, $C = 40$ pF, and different hit locations: $\diamond - M_1$; $\circ - M_5$; $\times - M_7$; $\square - M_9$ or M_{11}; $\triangle - M_3$.

the transconductor or DAC will ultimately generate a current pulse $i_{\rm se}$ flowing through one of the integrating capacitors (see Fig. 4). Because the duration of the single-event current pulse is short in comparison with the time constant associated to the output node of the integrator and it is restricted to a single clock cycle, one can approximate the change $v_{\rm se}$ in the output voltage as a step function. Therefore, we developed a single-event behavioral model for the integrator–DAC stage shown in Fig. 4(b). The amplitude of the perturbing voltage $v_{\rm se}$ depends on the amount of charge carried by the current pulse $i_{\rm se}$ and the value of the integrating capacitor.

To validate the single-event behavioral model of the integrator–DAC structure, transistor-level Hspice simulation have been carried out for several transconductor topologies. To achieve large SFDR, continuous-time Delta–Sigma modulators require highly linear transconductors. That is why only resistor-based OTA configurations have been considered [5]–[7] in our study. These designs have been transferred into a partially depleted 0.35 μm silicon-on-insulator (SOI) complementary metal–oxide–semiconductor (CMOS) process available from Honeywell. A simple SEE model for SOI metal–oxide–semiconductor field-effect transistors (MOSFETs) like the one proposed in [8] and [9] has been used to characterize the hits. In this model the SOI MOSFET is augmented with a double exponential pulse current source carrying a charge $Q_{\rm SEE}$. In our simulations every transistor in the studied circuits has been sequentially augmented with the SEE current source and transient simulations have been run for different values of $Q_{\rm SEE}$, ranging from 0.1pC to 1pC. The obtained results are similar for all considered transconductor topologies. Therefore, transient waveforms for only one configuration are presented next. Fig. 5 shows a $G_m - C$ integrator using the CMOS version of the OTA proposed in [5]. In Fig. 6 the output differential voltage of the integrator, $v_o = v_{o1} - v_{o2}$, is plotted for different hit transistors. From Fig. 6 one can see that the duration of the transient is less than 3 ns, being much smaller than the time constant associated with the output node of the integrator which is typically in the range of at least hundreds of microseconds. Furthermore, since for most applications of CMOS Delta–Sigma ADCs the sampling frequency is up to a couple of hundred megahertz, the SEE transient is also restricted to single clock cycle, validating the behavioral model proposed in Fig. 4(b).

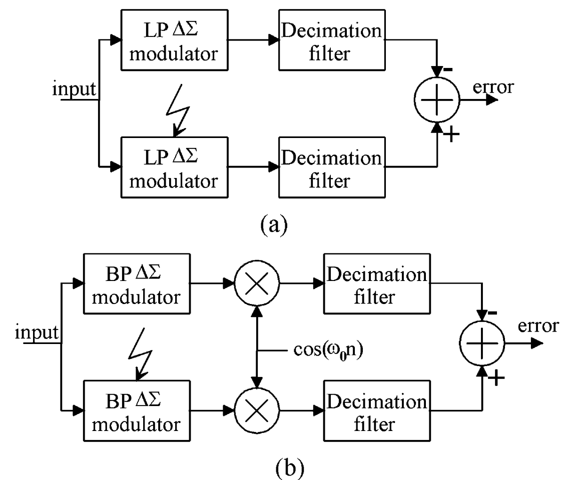

Fig. 7. SEE testing setup for Delta–Sigma ADCs.

In the case of the internal ADC, the SEE are much easier to characterize because they can only change the bit at the output of a comparator (SEU). This error propagates to the input of the subsequent digital decimation filter, but will also affect the value fed back by the DAC to the input of the modulator. Obviously, a one-bit Delta–Sigma modulator will be more sensitive to the SEU affecting the internal ADC because the energy carried by one bit (always the most significant bit) is large compared to the energy carried by one bit in the case of a multibit implementation. Moreover, bubble correction logic can be used to correct some of the errors affecting a multibit internal ADC.

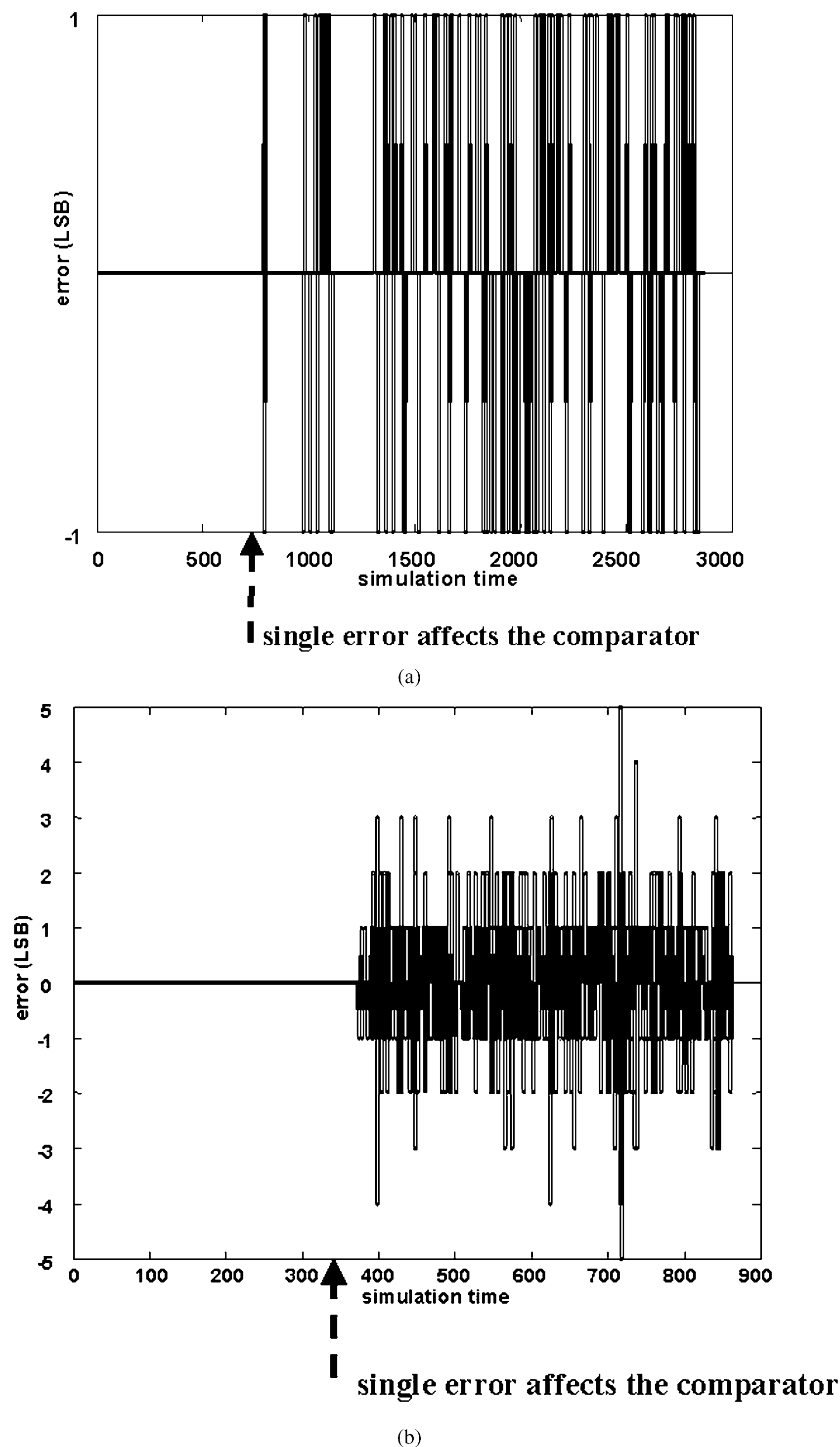

Fig. 8. Decimated output error induced by the SEU of the comparator: (a) low-pass case and (b) band-pass case.

III. Behavioral Simulation Results

A database of Simulink diagrams for several single-bit, single-loop Delta–Sigma modulators (both low-pass and band-pass) of different orders and topologies [1] has been developed. These ideal modulator diagrams have been augmented with blocks modeling the SEEs at the cell level and the setup depicted in Fig. 7 has been used to characterize the magnitude of the errors induced by SEEs. Two identical structures are driven by the same input signal, one of them being affected by single-event hits, and the other one assumed to operate in a radiation-free environment. Because we are interested only in characterizing the SEEs in the analog circuitry, it is assumed that the digital decimation filter is radiation hardened and no errors occur within. The output of the oversampling ADC affected by SEE is compared to the output of its error-free counterpart and the amplitude and duration of the SEE-induced error is measured. One has

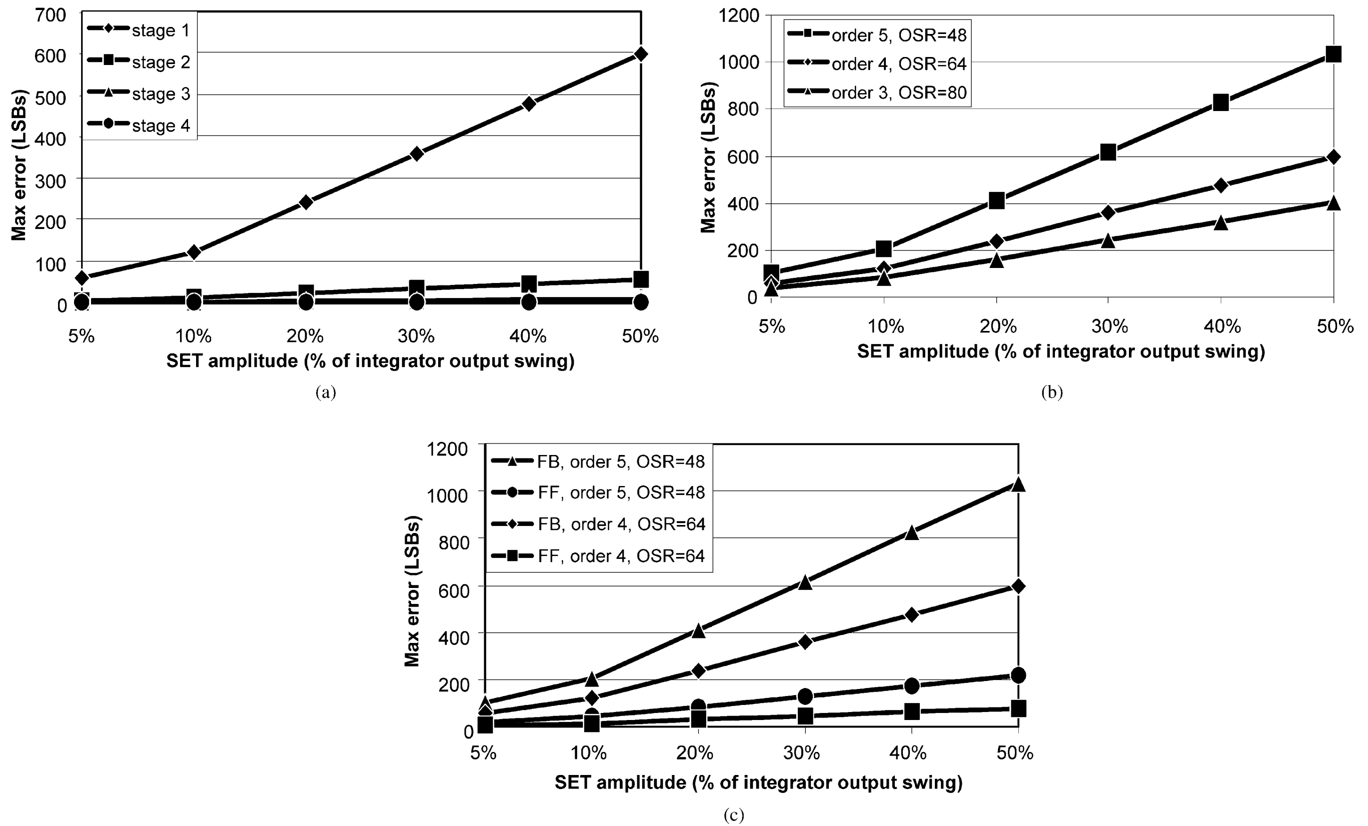

Fig. 9. Maximum error induced by SEE: (a) different hit locations; (b) different system parameters, same resolution; and (c) feedback versus feed-forward topologies.

to remark that one cannot compare directly the outputs of the modulators because of their inherent operation principle. Two different one-bit output streams can carry the same information of the input analog signal, the difference between the modulator outputs being the result of the random quantization error. Therefore, any small transient in one of the two modulators or a different initial condition in one of the integrating stages will cause a permanent divergence in their output signals, although the decimated outputs may not be affected. The setup for testing band-pass Delta–Sigma ADCs includes a digital mixer for down-converting the input modulated signals before the decimation filter. Because all tested band-pass modulator structures employ a center frequency equal to one fourth of the sampling frequency, the mixing operation reduces to multiplying the signal at the output of the modulator with the repeating sequence $(+1, 0, -1, 0)$.

For both low-pass and band-pass oversampling Delta–Sigma ADCs, the decimation filter has been implemented as a cascade between a finite impulse response (FIR) section with a $sinc^K$ type of frequency response, a down-sampling by (OSR/2) block, an infinite impulse response (IIR) filter with Butterworth frequency response, and a down-sampling by two block. The order of the FIR filter is large; therefore one can remark a delay between the SEE hit and moment the error occurs at the output. The effect of the IIR filter consists in propagating indefinitely very small errors at the decimated output. Therefore, errors of one least significant bit (LSB) will not be considered significant.

A. SEE Affecting the Internal ADC

In our simulations, only single-bit Delta–Sigma modulators have been considered. Fig. 8 shows two decimated error transients. If the output of the single-bit ADC is upset, affecting the output of the feedback DAC as well, the error at the output of the decimation filter is only ± 1 LSB (low-pass case) or up to ± 5 LSBs (band-pass case). The conclusion is that the internal ADC has no major influence on the decimated output, the error being slightly larger in the case of a band-pass modulator. We have also observed that the amplitude of the transients is independent of the oversampling ratio and/or order of the modulator. However, if the SEUs of the comparator occur when the input signal of the modulator is large, the modulator may become unstable.

B. SEE Affecting the Integrator–DAC Structure

If radiation single events occur at the integrator or feedback DAC level, the error at the decimated output is much larger and it can affect several output digital codes. Simulations have been carried out for:

- different values of v_{se} (normalized to the output voltage swing of the integrating stages);
- different orders of the modulators;
- different oversampling ratios;
- SEE affecting different integrating stages;
- different topologies of Delta–Sigma modulators;
- different input signal levels.

In Fig. 9(a) the effect of the hit location within the loop filter is depicted. The case of a feedback topology of order 4 and OSR = 64 is shown. As expected, the first integrating stage is the most critical one, whereas SEEs in subsequent stages are generating lower amplitude errors at the decimated output. In the following two plots only the results showing the effects of single-event hits in the first integrating stage will be presented, with these hits inducing to the largest errors. In Fig. 9(b) the maximum values of the error at the decimated output are plotted, for different orders and oversampling ratios of the modulator. The results obtained for the feedback topology are presented, with similar results being valid for the feed-forward topology. The chosen system parameters (order and OSR) achieve the same final resolution $N = 14$ bits. This plot shows that lower order and higher oversampling ratio offer better SEE immunity. In Fig. 9(c), a comparison between the feedback and feed-forward topologies is presented. One can see that the feed-forward topology is less sensitive to the SEE affecting the integrating stages. This can be explained by the fact that, for the same OSR, the gain of the first integrating stage of the feed-forward topology is larger than the one in the feedback topology. Therefore, the amplitude of the single-effect transient at the output of the first integrator is reduced more when reflected back at the global input of the modulator. These results allow us to determine the maximal error v_{se} affecting each integrating stage of a Delta–Sigma modulator, an error that does not decrease the overall resolution of the ADC below an imposed threshold. The maximal values of v_{se} sets the minimum value of the capacitors used in the integrating stages, and therefore the power consumption of the modulator.

IV. CONCLUSION

Single-event behavioral models for a class of analog cells used in continuous-time Delta–Sigma modulators are proposed. The validity of the proposed models has been verified by transistor-level simulations in Hspice. System-level behavioral simulations of SEEs in Delta–Sigma modulators have been carried out using Matlab's Simulink and the obtained results can be used to derive design parameters at the system level that will ensure an imposed radiation hardness. Although the presented results have been obtained in the case of continuous-time implementations of Delta–Sigma modulators, they can be easily extended to SC realizations. However, due to the sampling operation of such circuits, it is expected that the perturbing high-frequency components generated by the SEEs will be folded back into the baseband, and therefore decreasing the SEE immunity of the switched capacitor Delta–Sigma modulators.

REFERENCES

[1] S.R. Norsworthy, R. Schreier, and G.C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. Piscataway, NJ: IEEE Press, 1997.

[2] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of single-event transients in analog circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 2616–2623, Dec. 2000.

[3] O. Shoaei, "Continuous-time delta-sigma A/D converters for high-speed applications," Ph.D. dissertation, Carleton Univ., Ottawa, ON, Canada, 1996.

[4] L. J. Breems and J. H. Huijsing, *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*. Norwell, MA: Kluwer, 2001.

[5] S. D. Willingham, K. W. Martin, and A. Ganesan, "A BiCMOS low-distortion 8-MHz low-pass filter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1234–1245, Dec. 1993.

[6] A. Leuciuc and Y. Zhang, "A highly linear low-voltage MOS transconductor," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS 2002)*, vol. III, Phoenix, AZ, May 26–29, 2002, pp. 735–738.

[7] A. Worapishet and C. Naphaphan, "Current-feedback source-degenerated CMOS transconductor with very high linearity," *Electron. Lett.*, vol. 39, no. 1, pp. 17–18, Jan. 2003.

[8] S. E. Kerns, L. W. Massengill, D. V. Kerns, M. L. Alles, T. W. Houston, H. Lu, and L. R. Hite, "Model for CMOS/SOI single-event vulnerability," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 2305–2310, Dec. 1989.

[9] L. W. Massengill, E. V. Kerns, S. E. Kerns, and M. L. Alles, "Single-event charge enhancement in SOI devices," *IEEE Electron Device Lett.*, vol. 11, pp. 98–99, Feb. 1990.

[10] T. L. Turflinger, "Single-effect events in analog and mixed-signal integrated circuits," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 594–602, Apr. 1996.