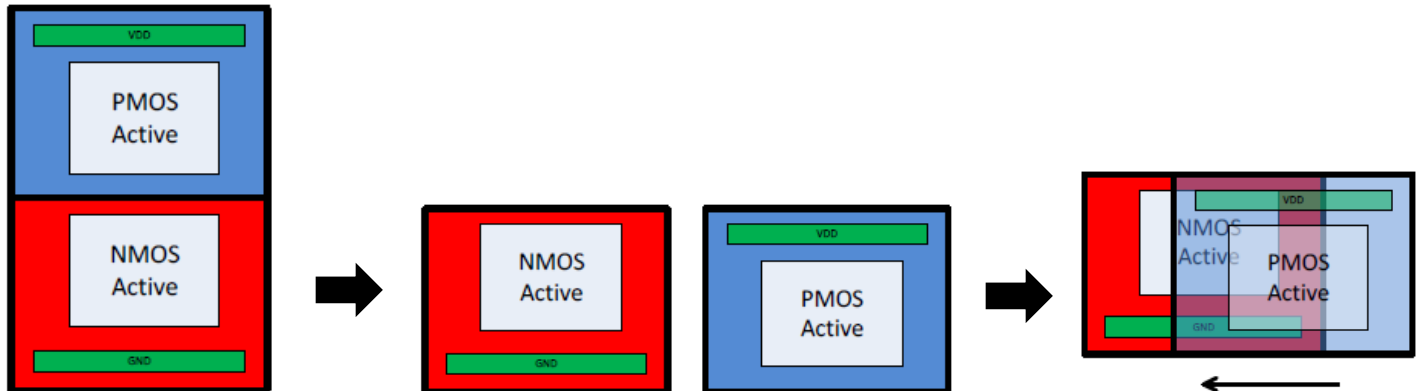


Technology: 45 nm (Based on NCSU FreePDK45)

*****Standard Cell*****

Cell layout methodology: Stacking



Cell Structure:

- Top Tier: NMOS, 10 metal layers (metal1 to metal10)
- Bottom Tier: PMOS, 5 metal layers (metal1_btm to metal5_btm)
- Tier connection: MIVs
 - MIV diameter: 100 nm
 - MIV resistance: 2 ohm
 - MIV capacitance: 0.1 fF
- Type of transistor used in layout: VTL

*****Standard Cell Library*****

Monolithic type: Transistor-level

Standard cell library generation tool: Cadence Encounter Library Characterizer (ELC)

Transistor model file used in ELC: *model_nom* from NCSU

Process Corner: typical

- Voltage: 1.1 v
- Temp: 27 C
- Vtn: 0.322v
- Vtp: 0.3021v