CURRICULUM VITAE

Emre Salman

ADDRESS

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RESEARCH INTERESTS

Analysis, modeling, and design methodologies for high performance digital and mixed-signal integrated circuits in both 2D and 3D technologies; energy efficient nanoscale circuits and systems; interconnect-centric design techniques to enhance performance, robustness, and reliability in monolithic, heterogeneous systems; and emerging integrated circuit and system technologies.

EDUCATION

- Ph. D. Electrical Engineering, 2006 – 2009, University of Rochester
  - Dissertation title: Switching Noise and Timing Characteristics in Nanoscale Integrated Circuits
  - Ph.D. Advisor: Eby G. Friedman
- M. S. Electrical and Computer Engineering, 2004 – 2006, University of Rochester
- B. S. Microelectronics Engineering, 1999 – 2004, Sabancı University

PROFESSIONAL EXPERIENCE

STONY BROOK UNIVERSITY
- Assistant Professor of Electrical and Computer Engineering, 2010 - present
- Director, Nanoscale Circuits and Systems (NanoCAS) Laboratory, 2011 - present

UNIVERSITY OF ROCHESTER
- Postdoctoral Research Associate, 2009 – 2010
- Instructor at Rochester Scholars Program, 2010
- Co-lecturer, Department of Electrical and Computer Engineering, 2009

FREESCALE SEMICONDUCTOR
- Research and Development Engineer, Summer 2006 and Summer 2007

SYNOPSYS
- Research and Development Engineer, Summer 2005

STMICROELECTRONICS
- Analog IC Design Engineer, 2003 - 2004

HONORS AND AWARDS

- National Science Foundation (NSF) CAREER Award, 2013
- Recipient, Outreach Initiative Fund, IEEE Circuits and Systems Society, 2012 and 2013
- Selected member of Rochester Scholars, sponsored by the University of Rochester, 2010
- Invited journal paper for IEEE Transactions on Circuits and Systems – I: Regular Papers, 2009
- Best paper nomination for IEEE International Symposium on Quality Electronic Design, 2005
- Recipient, Outstanding Senior Design Project Award, Sabancı University, 2004
- Recipient, full scholarship for undergraduate study, Sabancı University, 1999 – 2004

PUBLICATIONS

Book

1.E. Salman and E. G. Friedman, High Performance Integrated Circuit Design, Mc-Graw Hill, ISBN-10:0071635769, ISBN-13 978-0071635769, September 2012.

- Comprehensive tutorial book (17 chapters, 716 pages) that unifies interconnect-centric design methodologies in nanoscale ICs.

Journal Publications

2. S. M. Satheesh and E. Salman, ``Power Distribution in TSV Based 3D Processor-Memory Stacks,'' *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* Vol. 2, No. 4, pp. 692-703, December 2012.

3. E. Salman and E. G. Friedman, ``Utilizing Interdependent Timing Constraints to Enhance Robustness in Synchronous Circuits," *Microelectronics Journal*, Vol. 43, No. 2, pp. 119-127, February 2012.

4. S. Kose, E. Salman, and E. G. Friedman, ``Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) System*, Vol. 19, No. 8, pp. 1458-1468, August 2011.

5. E. Salman and Q. Qi, ``Path Specific Register Design to Reduce Standby Power Consumption," *Journal of Low Power Electronics and Applications*, Vol. 1, No. 1, pp. 131-149, April 2011.

6. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, ``Methodology for Efficient Substrate Noise Analysis in Large Scale Mixed-Signal Circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1405-1418, October 2009.

7. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, ``Identification of Dominant Noise Source and Parameter Sensitivity for Substrate Coupling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 10, pp. 1559-1564, October 2009.

8. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, ``Worst Case Power/Ground Noise Estimation Using an Equivalent Transition Time for Resonance," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 56, No. 5, pp. 997-1004, May 2009.

9. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, ``Exploiting Setup-Hold Time Interdependence In Static Timing Analysis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 6, pp. 1114-1125, June 2007.

Refereed Conference Publications

10. H. Wang, M. H. Asgari, and E. Salman, "Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, (to appear), May 2013.

11. S. M. Satheesh and E. Salman, "Effect of TSV Fabrication Technology on Power Distribution in 3D ICs," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, (to appear), May 2013.

12. H. Wang and E. Salman, "Power Gating Topologies in TSV Based 3D Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, (to appear), May 2013.

13. S. M. Satheesh and E. Salman, "Design Space Exploration for Robust Power Delivery in TSV Based 3D Systems-on-Chip," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 307-311, September 2012.

14. Z. Gan, E. Salman, and M. Stanacevic, "Methodology to Determine Dominant Noise Source in a System-on-Chip Based Implantable Device," *Proc. of the IEEE International System-on-Chip Conference***,** pp. 115-119, September 2012.

15. E. Salman, M. H. Asgari, and M. Stanacevic, "Signal Integrity Analysis of a 2D and 3D Integrated Potentiostat for Neurotransmitter Sensing," *Proc. of the IEEE Biomedical Circuits and Systems Conference*, pp.17-20, November 2011.

16. G. Bischof, B. Scholnick, and E. Salman, "Fully Integrated PLL Based Clock Generator for Implantable Biomedical Applications," *Proc. of the IEEE Annual Conference on Long Island Systems, Applications and Technology*, May 2011.

17. E. Salman, "Noise Coupling Due to Through Silicon Vias (TSVs) in 3D Integrated Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1411-1414, May 2011.

18. E. Salman, "Noise Management in Highly Heterogeneous SoC Based Integrated Circuits," *Proceedings of the IEEE International SoC Design Conference*, pp. 1-4, November 2010 (Invited paper).

19. R. Secareanu, O. Hartin, J. Feddeler, R. Moseley, J. Shepherd, B. Vrignon, J. Yang, Q. Li, H. Zhao, W. Li, L. Wei, E. Salman, R. Wang, D. Blomberg, and P. Parris, "Impact of Low-Doped Substrate Areas on the Reliability of Circuits Subject to EFT Events," *Proceedings of the IEEE International SoC Design Conference*, pp. 21-24, November 2010.

20. R. Jakushokas, E. Salman, E. G. Friedman, R. M. Secareanu, O. L. Hartin, and C. Recker, "Compact Substrate Models for Efficient Noise Coupling and Signal Isolation Analysis," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2346-2349, May/June 2010.

21. E. Salman and E. G. Friedman, "Methodology to Achieve Higher Tolerance to Delay Variations in Synchronous Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 447-452, May 2010.

22. E. Salman and E. G. Friedman, "Reducing Delay Uncertainty in Deeply Scaled Integrated Circuits Using Interdependent Timing Constraints," *Proceedings of the ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pp. 77-82, March 2010.

23. Kose, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277-2280, May 2009.

24. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Contact Merging Algorithm for Efficient Substrate Noise Analysis in Large Scale Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 9-14, May 2009.

25. S. Kose, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 47-50, September 2008.

26. E. Salman and E. G. Friedman, "Methodology for Placing Localized Guard Rings to Reduce Substrate Noise in Mixed-Signal Circuits," *Proc. of the 4th Conf. on PhD Research in Microelectronics and Electronics*, pp. 85-88, June 2008.

27. E. Salman, R. Jakushokas, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Input Port Reduction for Efficient Substrate Extraction in Large Scale IC's," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 376-379, May 2008.

28. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Equivalent Rise Time for Resonance in Power/Ground Noise Estimation," *Proc. of the IEEE International Symposium on Circuits and System*, pp. 2422-2425, May 2008.

29. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates," *Proc. of the IEEE Int. Symposium on Quality Electronic Design*, pp. 261-266, March 2008.

30. E. Salman, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Substrate Noise Reduction Based On Noise Aware Cell Design," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 3227-3230, May 2007 (Invited paper).

31. E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 293-296, September 2006.

32. E. Salman, A. Dasdan, F. Taraporevala, K. Kucukcakar, and E. G. Friedman, "Pessimism Reduction in Static Timing Analysis Using Interdependent Setup and Hold Times," *Proceedings of the IEEE International Symposium on Quality Electronic Design*, pp. 159-164, March 2006 (Nominated for the best paper award).

33. E. Salman, H. Akin, O. Gursoy, A. Ergintav, I. Tekin, A. Bozkurt, and Y. Gurbuz, "Design of a 3.2 mW PLL Based Clock and Data Recovery Circuit in 90-nm CMOS Technology," *Proceedings of the Mediterranean Microwave Symposium*, September 2005.

Patents

34. A. Dasdan, E. Salman, F. Taraporevala, and K. Kucukcakar, "Characterizing Sequential Cells Using Interdependent Setup and Hold Times, and Utilizing the Sequential Cell Characterization in Static Timing Analysis", US Patent No 7,506,293.

35. R. M. Secareanu, O. L. Hartin, and E. Salman "Apparatus and Method For Reducing Noise in Mixed-Signal Circuits and Digital Circuits", US Patent No 7,834,428

PROFESSIONAL ACTIVITIES

- Associate editor, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2011 to present
- Associate editor, *Journal of Circuits, Systems and Computers*, 2010 to present
- Associate editor, *Journal of Low Power Electronics and Applications*, 2010 to present
- Publicity chair, DAC PhD Forum, 2012
- Technical program committee member, First International Workshop on Secure and Resilient Architectures, 2012
- Technical program committee member, ACM Great Lakes Symposium on VLSI, 2010, 2011, 2012, 2013
- Technical program committee member, Asia Symposium on Quality Electronic Design, 2011, 2012
- Technical program committee member, International Symposium on Electronic System Design, 2011, 2012
- Technical program committee member, The First International IEEE Workshop on Thermal Modeling and Management: Chips to Data Centers, 2011
- Technical program committee member, IEEE International Conference on Microelectronics, 2011, 2012
- Session chair, Sensors, IEEE International Symposium on Circuits and Systems, 2012
- Session chair, Nanorobotics and Nano-Giga Circuits, IEEE International Symposium on Circuits and Systems, 2011
- Session chair, VLSI Circuits, ACM Great Lakes Symposium on VLSI, 2010
- Instructor at Engineering Summer Camp for high school students, Stony Brook University, Summer 2012
- Instructor at Rochester Scholars Program for high school students, University of Rochester, Spring 2010
- Technical judge at the WAC Foundation Invitational Science Fair, Long Island, 2011 and 2012
- Member, IEEE (since 2002), Circuits and Systems Society

INVITED TALKS

1. Robust Power Delivery in TSV Based 3-D Processor-Memory Stacks, *CASS Forum on Emerging and Selected Topics (CAS-FEST)*, Heterogeneous Nano-Circuits and Systems, Seoul, South Korea, May 2012.
2. Noise Management in Highly Heterogeneous SoC Based Integrated Circuits, *IEEE International SoC Design Conference*, Seoul, South Korea, November 2010.
3. Noise-Centric Physical Design Methodologies for VLSI Based Nanoscale Systems, March-April 2010.
    - Stony Brook University, Stony Brook, NY
    - University of Pittsburgh, Pittsburgh, PA
    - University of Miami, Miami, FL
    - University of Alaska at Fairbanks, Fairbanks, AK
    - University of Maryland at Baltimore County, Baltimore, MD
4. Switching Noise and Timing Considerations in Nanoscale Integrated Circuits, *Microelectronics Group, Sabancı University*, Istanbul, June 2008.
5. Substrate Noise Reduction Based on Noise Aware Cell Design, *IEEE International Symposium on Circuits and Systems*, New Orleans, LA, May 2007.
6. Impact of Substrate on Ground Noise, *Microwave and Mixed-Signal Technologies Laboratory, Freescale Semiconductor*, Tempe, AZ, February 2006.

TEACHING ACTIVITY

- Spring 2013: ESE 324 Electronics Laboratory C (55 students) and ESE 585: Nanoscale Integrated Circuit Design (29 students)
- Fall 2012: ESE 555 Advanced VLSI Systems Design (61 students)
- Spring 2012: ESE 324 Electronics Laboratory C (47 students)
- Fall 2011: ESE 555 Advanced VLSI Systems Design (47 students)
- Spring 2011: ESE 324 Electronics Laboratory C (47 students)
- Fall 2010: ESE 670 High Performance Integrated Circuit Design in the Nanoscale Era (10 students)

UNIVERSITY AND DEPARTMENTAL SERVICE

- Graduate admissions committee, 2011, 2012, 2013
- Undergraduate advising committee for Computer Engineering, 2011, 2012, 2013
- Co-director, Engineering Summer Camp, 2013
- Instructor at Engineering Summer Camp, 2012
- Assessment committee chair for ESE 324

UNDERGRADUATE RESEARCH ACTIVITY

1. Jongmun Hwang, 2012-2013
2. Artem Ayzen, 2011-2012
3. Garrett Bischoff, 2010-2011
4. Ben Scholnick, 2010-2011

CURRENT GRADUATE STUDENTS

1. Zhihua Gan (Ph.D.)
2. Peirong Ji (Ph.D.)
3. Hailang Wang (Ph.D.)
4. Ajay Chandrasekhar (M.S.)
5. Sateja Mungi (M.S.)
6. Ziqi Zhang (M.S.)

PAST GRADUATE STUDENTS

1. Mohammad H. Asgari, M.S. degree in 2011, currently Ph.D. student at Columbia University
2. Suhas M. Satheesh, M.S. degree in 2012, currently IC design engineer at NVIDIA