Effect of TSV Fabrication Technology on Power Distribution in 3D ICs

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ABSTRACT

The design implications of two distinct through silicon via (TSV) fabrication methods (via-first and via-last) have been investigated for power delivery in a 3D system. Different geometry, connectivity, and filling materials have been considered to develop equivalent electrical models for both via-first and via-last based power distribution networks. Based on these models, a valid design space has been developed where power supply noise is satisfied and physical area overhead is minimized. Under constant power supply noise, a via-last based power network occupies 7.5% less area. However, in addition to causing routing blockages, a via-last based power network exhibits high sensitivity to design parameters due to a high quality factor. Alternatively, a via-first based power network requires a large number of TSVs, but exhibits relatively more predictable behavior due to a lower quality factor (higher damping).

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]:

General Terms

Design; 3D IC; TSV; Power noise

1. INTRODUCTION

Three-dimensional (3D) integration is an emerging paradigm for developing multi-functional systems at a lower cost. Utilizing the vertical dimension not only increases the integration density, but also reduces the length and number of global interconnects. This reduction enhances system performance (due to reduced interconnect delay) while lowering the power consumption (due to reduced switching capacitance) [1–3]. Furthermore, through silicon via (TSV) based 3D technologies enable heterogeneous integration that expands the application domain from high performance computing to relatively lower power systems-on-chip consisting of, for example, sensors, analog/RF circuits, memory, and digital processing blocks, as depicted in Fig. 1.

A significant circuit- and physical-level challenge in 3D ICs is reliable power delivery to each plane. Maintaining the power supply voltage variations within 5-10% of the global V_{DD} is highly challenging due to three reasons [4]: 1) higher supply current, 2) lower supply voltage around or below one volt, and 3) relatively high TSV impedances that vary depending upon the particular TSV fabrication method.

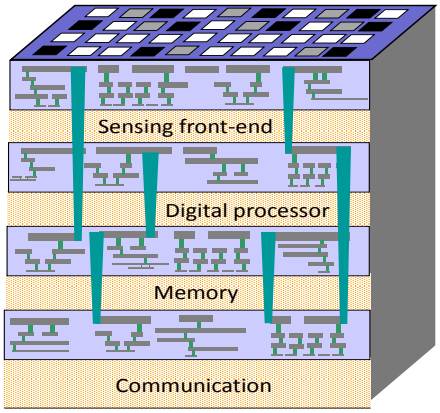

Figure 1: Three-dimensional integration of diverse planes using through silicon via technology [1].

Previous works on 3D power delivery have focused on different power distribution topologies, effect of TSV geometry, and 3D decoupling capacitor placement techniques [5–7]. A primary limitation of the existing works is the absence of a strong link between proposed design guidelines and distinct TSV fabrication methods. Each TSV technology exhibits unique characteristics, thereby requiring different design constraints. Pavlidis and De Micheli have demonstrated the advantage of alternative low impedance current paths in via-first TSVs [8]. These additional current paths have been exploited, resulting in a 22% reduction in the number of intraplane vias or alternatively, a 25% decrease in the required decoupling capacitance. Different filling materials for via-first and via-last TSVs, however, have not been considered. Furthermore, a simplified model has been assumed for the power distribution network within each plane.

The primary contributions of this paper are three-fold: (1) electrical characteristics and connectivity differences of via-first and via-last TSVs are considered during the design process of a robust 3D power distribution network. (2) Design space that satisfies power supply noise while minimizing the physical area is determined for both via-first and via-last TSVs. Note that area overhead is an important concern in TSV based 3D ICs, particularly for low power, low cost applications. (3) Related tradeoffs are identified both at the fabrication and circuit levels, providing design guidelines in developing 3D power networks.

The rest of the paper is organized as follows. The characteristics

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Table 1: Characteristics of via-first and via-last TSVs [9–11].

Parameter	Via-first	Via-last
Filling material	Doped polysilicon	Copper
Processing temperature	High	Low
Sensitivity to contamination	Low	High
Manufacturability	Difficult	Established
Formation	Before FEOL	After BEOL
Electrical characteristics	Highly resistive	Inductive
Landing metal	M_1	M_{Top}
Take-off metal	M_{Top}	M_{Top}

of the via-first and via-last technologies are reviewed in Section 2. Electrical models for 3D power distribution for both technologies are described in Section 3. The results of the proposed analysis are provided in Section 4, and the paper is concluded in Section 5.

2. PRIMARY CHARACTERISTICS OF TSV TECHNOLOGIES

Each TSV technology exhibits unique challenges in designing a 3D power distribution network. These differences arise due to distinct fabrication techniques. The fabrication characteristics and relative physical dimensions of via-first and via-last TSVs are summarized, respectively, in Sections 2.1 and 2.2. These properties are also listed in Table 1.

2.1 Via-First TSV

In the via-first method, TSVs are fabricated before the transistors are patterned in silicon, *i.e.*, prior to front-end-of-line (FEOL) [9, 10]. Thus, TSVs fabricated with the via-first technique do not pass through the metalization layers, as depicted in Fig. 2. This characteristic is an important design advantage since via-first TSVs do not affect the routability of the signals. In via-first technology, the TSV of a plane is connected between the first metal layer of the current plane and the top most metal layer of the previous plane. Polysilicon is typically used as the filling material due to its ability to withstand high temperatures [9, 10]. Via-first TSVs are less sensitive to contamination since both the filling and substrate material are the same [10]. The physical dimensions of via-first TSVs are smaller than via-last TSVs [11]. Via-first TSVs, however, are highly resistive due to the use of polysilicon as the filling material.

2.2 Via-Last TSV

In the via-last approach, TSV formation occurs after the metalization layers are fabricated, *i.e.*, after BEOL [9–11]. Thus, as opposed to via-first TSVs, via-last TSVs pass through the metal layers, causing metal routing blockages, as depicted in Fig. 2 [8, 11]. A lower resistivity filling material such as copper is used since high temperature FEOL and BEOL processes are performed before the via formation [9, 10]. The use of copper as a filling material makes the process sensitive to both temperature (must be maintained less than 230°C) and contamination [10]. Despite exhibiting relatively low resistance, the inductive characteristics of via-last TSVs are relatively more significant than via-first TSVs due to greater physical dimensions [11]. The physical connection between the TSV and metal layers is typically achieved at the top most metal layer.

3. ELECTRICAL MODELS FOR 3D POWER DISTRIBUTION

The models that are used to analyze power supply noise for each TSV technology are described in this section. System level model, including the orientation of the planes and the dimensions of the dies are discussed in Section 3.1. Electrical models used for TSVs, substrate, and the power distribution network within a plane are provided, respectively, in Sections 3.2, 3.3, and 3.4. Finally, the model for the load circuit is described in Section 3.5.

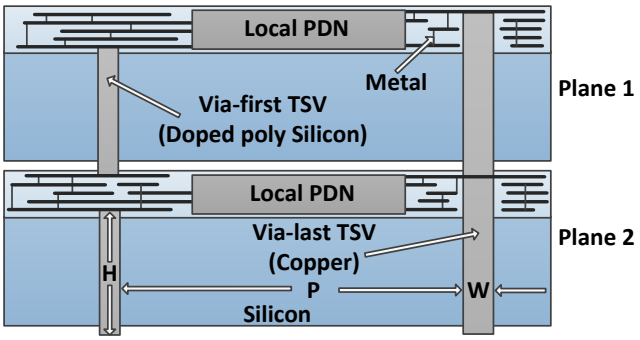

Figure 2: Illustration of via-first and via-last TSV fabrication technologies.

3.1 System Level Model

A 3D system in 32 nm CMOS technology consisting of eight memory planes and one plane for the processor core is considered. The power supply voltage V_{DD} is equal to 1 volt. Devices in each plane occupy an area of 120 mm^2. The system has 1 (gigabyte) GB of DRAM spread uniformly across eight memory planes. Each memory plane has 1 (gigabit) Gb DRAM. Every plane is divided into 32 modules of equal size. Each of these modules consumes an area of 1500×2500 μm^2. This topology is depicted in Fig. 3. For via-first technology, the TSVs are placed beneath the active circuit, as illustrated in Fig. 3(a) whereas in via-last technology, the power and ground TSVs are distributed on both sides of each module, as depicted in Fig. 3(b). Note that although the TSVs are placed beneath the active circuit in via-first technology, these TSVs consume additional device area. Thus, in Fig. 3(a), the area represented by each DRAM module includes both the 1500×2500 μm^2 DRAM area and the TSV area. A nine metal layer process is considered where the metal thickness and aspect ratio are determined according to an industrial 32 nm CMOS technology [12].

The processor plane is closest to the heat sink and farthest from the package due to its high switching activity. The orientation of the memory planes such as face-to-face or face-to-back exhibits a design tradeoff. The first memory plane can face the package where the metal layers are directly connected without the TSVs to the package pads or it can face the adjacent DRAM plane. In the second option, as considered in this work, TSVs are required to connect the first memory plane with the package pads. First option eliminates these TSVs, but the additional current paths available in via-first technology [8] cannot be exploited in distributing power. These additional current paths exist only when the current flow is from the lowest to the highest metal layer in a plane. Another consideration is the orientation between the processor plane and the adjacent memory plane. A face-to-back approach maintains the symmetry of the 3D system, but the communication bandwidth between the two planes is limited. Alternatively, in a face-to-face approach, processor and memory can communicate with the metal layers without requiring TSVs, thereby enhancing the communication bandwidth. This scheme, as considered in this work, also reduces the overall number of TSVs, compensating the additional TSVs between the first memory plane and package. Thus the processor plane does not house any TSVs. The 3D processor-memory

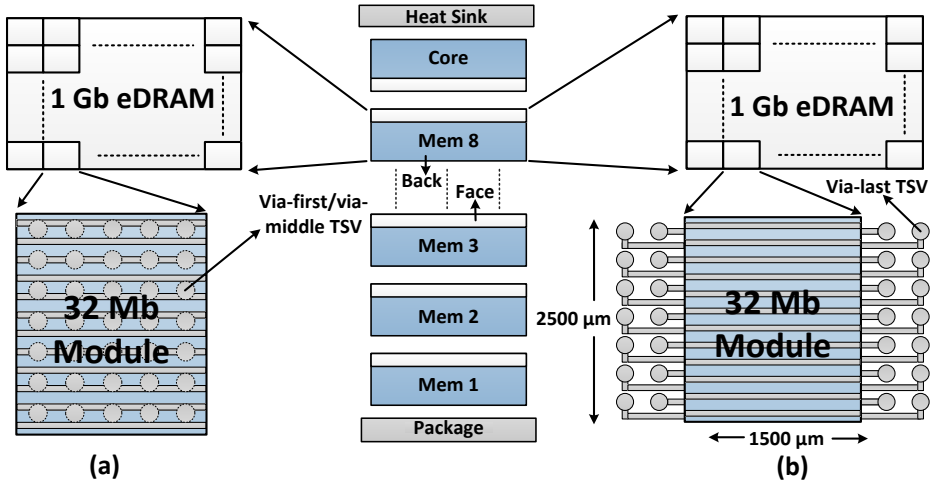

Figure 3: Illustration of the 3D processor-memory stack: (a) via-first TSVs and (b) via-last TSVs.

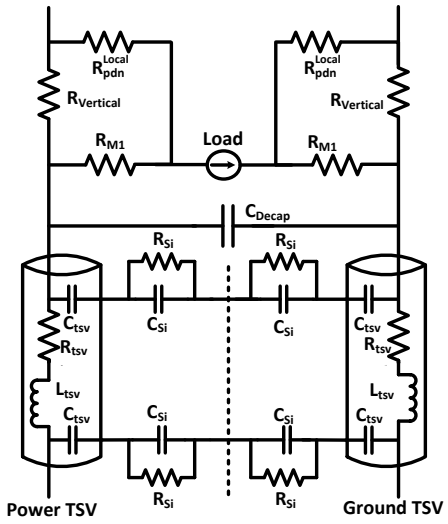

Figure 4: Equivalent power distribution network.

stack is illustrated in Fig. 3. The parasitic package resistance and inductance are, respectively, 3 mΩ and 100 pH at both the power and ground supplies.

In the rest of this paper, the analysis is performed for an area of $1500 \times 2500\ \mu m^2$, which corresponds to one of the 32 modules. The procedure is similar for the remaining 31 modules. All of the references to the amount of decoupling capacitance represent the capacitance in each module. Similarly, a reference to the number of TSVs represents the number of power TSVs in each module. An equivalent electrical model corresponding to the power distribution network of this portion of the system is illustrated in Fig. 4. This model consists of the TSVs, substrate, power distribution network within a plane, switching load circuit, and decoupling capacitance, as described in the following sections.

3.2 TSV Model

A TSV is typically represented as a cylinder with a diameter W and depth H. Aspect ratio of a TSV is given by H/W. The minimum distance between the two TSVs is determined by the pitch P, which is typically twice the TSV diameter. The TSV model consists of a resistance R_{tsv} and inductance L_{tsv} due to the filling material, and a capacitance to the substrate C_{tsv} due to the thin dielectric layer [13]. R_{tsv} is determined by [14],

$$R_{tsv} = \sqrt{(R_{AC}^{tsv})^2 + (R_{DC}^{tsv})^2}, \tag{1}$$

where the DC resistance R_{DC}^{tsv} and AC resistance R_{AC}^{tsv} are, respectively,

$$R_{DC}^{tsv} = \frac{\rho_f H}{\pi (W/2)^2}, \tag{2}$$

$$R_{AC}^{tsv} = \frac{\rho_f H}{2\pi (W/2)\delta_{tsv}}. \tag{3}$$

ρ_f is the conductivity of the filling material and the skin depth δ_{tsv} is [14]

$$\delta_{tsv} = \frac{1}{\sqrt{\pi f \mu_f \rho_f}}, \tag{4}$$

where f is the frequency and μ_f is the permeability of the filling material. The TSV inductance L_{tsv} is [15]

$$L_{tsv} = \frac{\mu_o}{4\pi}[2H \ln(\frac{2H + \sqrt{(W/2)^2 + (2H)^2}}{W/2}) + (W/2 - \sqrt{(W/2)^2 + (2H)^2})], \tag{5}$$

where μ_o is vacuum permeability. The TSV capacitance C_{tsv} is determined from the cylindrical capacitor formula as [16]

$$C_{tsv} = \frac{2\pi \varepsilon_{ox} H}{\ln(\frac{W/2 + t_{ox}}{W/2})}, \tag{6}$$

where ε_{ox} is the oxide permittivity. Note that the skin effect is neglected for via-first TSVs due to its sufficiently small TSV diameter. The primary characteristics of the two TSV technologies are also listed in Table 2.

3.3 Substrate Model

The substrate is modeled as an *RC* impedance, where substrate capacitance, C_{si}, and substrate resistance, R_{si} are, respectively [16],

$$C_{si} = \frac{\pi \varepsilon_{si} H}{\ln\left(\frac{2P}{W/2} + \sqrt{(\frac{2P}{W/2})^2 - 1}\right)}, \tag{7}$$

Table 2: Model parameters for TSVs [9, 15].

Parameter	Via-first	Via-last
Diameter W	4 μm	10 μm
Height H	10 μm	60 μm
Pitch P	8 μm	20 μm
Oxide thickness t_{ox}	0.2 μm	0.2 μm
TSV resistance R_{tsv}	5.7 Ω	20 mΩ
TSV inductance L_{tsv}	4.18 pH	34.94 pH
TSV capacitance C_{tsv}	23 fF	283 fF
Aspect ratio AR	2.5:1	6:1
Material resistivity ρ_f	7.2 $\mu\Omega$m	16.8 nΩm
Substrate resistance R_{si}	8.81 kΩ	1.76 kΩ
Substrate capacitance C_{si}	1.19 fF	6 fF
Co-efficient of thermal expansion CTE	Low	17 ppm/K

Table 3: Power distribution network resistances within a plane.

Parameter	Via-first	Via-last
Network resistance R_{pdn}^{Local}	1.97 mΩ	8.51 mΩ
Vertical resistance $R_{Vertical}$	1.97 mΩ	NA
M1 Path Resistance R_{M1}	73 $\mu\Omega$	∞

$$R_{si} = \frac{\varepsilon_{si}\rho_{si}}{C_{si}}. \quad (8)$$

where $\varepsilon_{si} = 105 \times 10^{-12}$ F/m and $\rho_{si} = 10$ Ωcm are, respectively, silicon permittivity and substrate resistivity. These numbers are listed in Table 2.

3.4 Plane-Level Power Distribution Network

As shown in Fig. 2, in the via-first method, local metal layers are utilized to connect the two TSVs located in adjacent planes whereas via-last based TSVs pass through the metal layers. As depicted in Fig. 4, the local power network is modeled with three resistances, which are determined based on 32 nm technology parameters [12]. An interdigitated grid topology is adopted where a stack of vias, located at each intersection of M_9 and M_8, transmits the power supply voltage down to the first metal layer, and eventually to the switching transistors. A single stack of vias from M_1 to M_9 has 16 Ω resistance [17]. Note however that there is a large number of parallel paths. The value of resistances in Fig. 4 resulting from simulation results are listed in Table 3.

3.5 Switching Circuit

The switching circuit for both memory and processor is modeled as a piecewise linear current source, as shown in Fig. 5. The DRAM consumes 3 W of power uniformly distributed across the eight stacks [5]. Alternatively, the processor consumes 90 W of power. 30% of the overall power is due to static power dissipation whereas the remaining portion is due to dynamic power consumption [5]. As illustrated in Fig. 5, a triangular current waveform is assumed. The DC current I_{dc} and peak current I_{peak} are determined based on, respectively, the static and dynamic power consumption. The power and switching current characteristics for the DRAM and

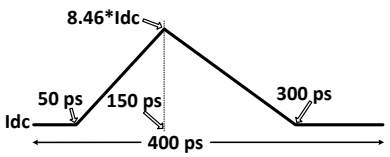

Figure 5: Piecewise linear current source model to mimic switching circuit.

Table 4: Power parameters used to estimate the characteristics of switching current [5].

Parameter	DRAM	Processor
Total power	3 W	90 W
Static Power	0.9 W	27 W
Dynamic Power	2.1 W	63 W
Static Current	28.125 mA	843.75 mA
Peak Current	238.125 mA	7.14 A
Operating Frquency	2.5 GHz	2.5 GHz

the processor are listed in Table 4. Note that the power characteristics in this table are for the entire system whereas the current characteristics represent the current in each of the 32 modules.

4. SIMULATION RESULTS

The dependence of peak noise on decoupling capacitance and number of TSVs, design space that satisfies the target power supply noise, and the area overhead due to TSVs and decoupling capacitance are provided in this section. The power supply noise is observed across the current source located at the processor plane which is the farthest node from the power supply pads. In transient analysis, the tolerable power supply noise is assumed to be 100 mV at the power and ground planes. Decoupling capacitance is implemented using MOS capacitors in an industrial 32 nm technology node with a capacitance density of 39.35 fF/μm^2 as determined from the equivalent oxide thickness (EOT) of the technology [12]. Results for via-first and via-last technologies are discussed, respectively, in Sections 4.1 and 4.2.

4.1 Via-First TSV

Use of doped polysilicon as the filling material in via-first technology causes the TSVs to be highly resistive. Shorter TSV height makes via-first TSVs relatively less inductive. Due to these two reasons, a via-first based power network is typically over-damped.

4.1.1 Valid Design Space to Satisfy Target Power Supply Noise

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 6(a) for via-first TSVs. Since the power distribution network is over-damped, the response is monotonic. Thus, peak noise decreases as the number of TSVs and/or decoupling capacitance increase. To determine the valid design space, a contour at 100 mV peak noise is extracted from the noise surface, as depicted in Fig. 6(b). Any point above the curve satisfies the noise constraint whereas the shaded region should be avoided.

4.1.2 Optimum Number of TSVs and Decoupling Capacitance

Since multiple valid pairs of number of TSVs and decoupling capacitance exist, a pair that minimizes the overall area overhead can be chosen. The area overhead is depicted in Fig. 7 for each point on the contour of Fig. 6(b). As demonstrated in this figure, a specific design point exists that minimizes the area overhead. This design point corresponds to 2750 TSVs and 2.7 nF of decoupling capacitance, producing an area overhead of approximately 9%. Note that if an arbitrary pair is chosen from the contour in Fig. 6(b), the area overhead can be as high as 16%.

An important design requirement is to have a significantly high number of via-first TSVs to reduce current per TSV, which increases the required physical area. Note however that 6.25 times more via-first TSVs than via-last TSVs can be placed within a given area due to smaller via-first TSV dimensions. Also note that a large

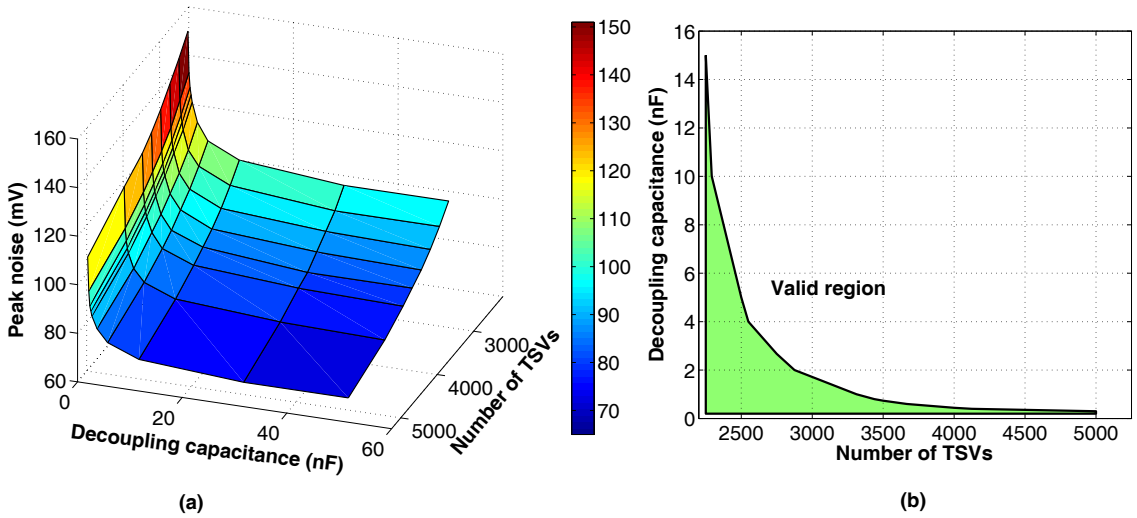

Figure 6: Peak noise as a function of number of via-first TSVs and decoupling capacitance: (a) surface plot and (b) contour plot at 100 mV.

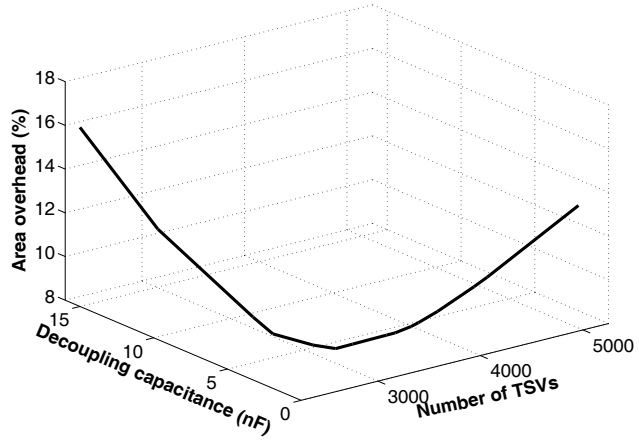

Figure 7: Area overhead in via-first technology.

amount of decoupling capacitance is required to reduce transient *IR* noise. An advantage of a via-first based power distribution network is the high damping factor due to high TSV resistance and low TSV inductance. Thus, decoupling capacitance effectively suppresses the transient noise, producing a low peak-to-peak noise, as listed in Table 5.

4.2 Via-Last TSV

Via-last TSV technology exhibits significantly different noise characteristics as compared to via-first TSV technology due to differences in filling material and physical dimensions. Due to significantly less resistance and a relatively large inductance, a power distribution network with via-last TSVs is typically under-damped.

4.2.1 Valid Design Space to Satisfy Target Power Supply Noise

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 8(a) for via-last TSVs. As opposed to via-first TSVs, the noise surface is non-monotonic with multiple peaks where the noise exceeds the design objective. The noise contour at 100 mV is illustrated in Fig. 8(b) to determine the valid design space where the peak noise constraint is satisfied. The unshaded region represents a valid combination of number of TSVs and decoupling capacitance. As illustrated in this figure, at a specific decoupling capacitance, an increase in the number of TSVs can violate the noise constraint due to a lower damping factor. In via-last technology, the power supply noise is highly sensitive to number of TSVs and decoupling capacitance, particularly at relatively low decoupling capacitances. Furthermore, peak-to-peak noise is also significantly higher, as listed in Table 5.

Table 5: Valid design space that satisfies the power supply noise while minimizing physical area.

TSV type	Area penalty	Number of TSVs	Decoupling capacitance (nF)	Peak-to-peak noise (mV)
Via-first	9.06%	2750	2.7	33.42
Via-last	1.54%	76	0.385	134.72

4.2.2 Optimum Number of TSVs and Decoupling Capacitance

The area overhead, however, is significantly lower in via-last TSVs since the number of required TSVs is less. The dependence of area overhead on number of TSVs and decoupling capacitance for the valid design points are represented in Fig. 9. Note that this relationship is highly complicated due to the non-monotonic behavior of the power supply noise. This behavior suggests that it is highly critical to appropriately choose the number of TSVs and amount of decoupling capacitance in a via-last based power network. The design points that correspond to the minimum area overhead while satisfying the power supply noise are listed in Table 5.

5. CONCLUSIONS

Distinct design requirements of via-first and via-last TSVs have been identified for robust power delivery in 3D ICs. Electrical models have been developed considering different connectivity characteristics, physical geometry, and filling materials. A valid design space that satisfies target power supply noise while minimizing physical area has been identified for both TSV technologies assuming a 32 nm processor-memory stack. Despite the low parasitic resistance of via-last TSVs, a power network based on via-last TSVs produces signal routing blockages and exhibits high inductive behavior, thereby producing a non-monotonic design space. Thus, the power network exhibits high sensitivity to design parameters. Alternatively, a power network based on via-first TSVs is typically

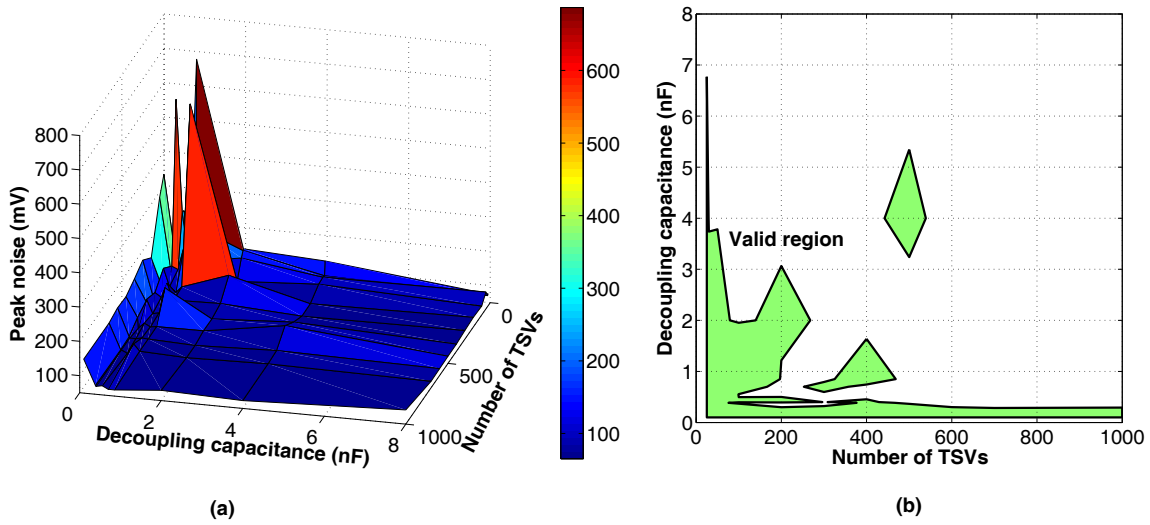

Figure 8: Peak noise as a function of number of via-last TSVs and decoupling capacitance: (a) surface plot and (b) contour plot at 100 mV.

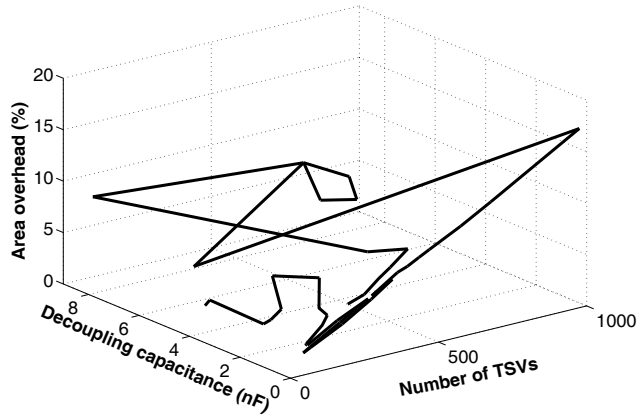

Figure 9: Area overhead in via-last technology.

over-damped, producing a monotonic and more predictable design space. Due to high TSV resistance, a via-first based power network can satisfy the power supply noise at the expense of 7.52% additional area overhead.

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