# MOHIT ARORA

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## Summary:


MSEE graduate seeking ASIC, FPGA or SoC Design Verification Position. Experience with RTL Design and Verification using Verilog, System Verilog and HVL methodologies.


## Technical Skills:

- HDL Languages: **Verilog, System Verilog, Basic UVM.**
- Programming Languages: C, C++, Unix/Linux Basic, Assembly Language Programming.
- Scripting: **Perl,** Shell.
- Programming and Designing Tools: **ModelSim, Questasim,** Cadence-Virtuoso, MATLAB.
- Operating System: Windows, Linux/Unix.
- Applications: Adobe Photoshop, Visual Basic, MS Office, Power Point, Avery, Excel.

## Education & Work Experience:

**Dec, 2013** State University of New York at Stony Brook, USA.
**Masters of Electrical Engineering** **GPA (3.83)**

**Nov, 2013** **Verifast Technologies, San Jose, CA, USA.** **TRAINING (4months)**

- **UART Interface Testing Project. –Tools used: Verilog, System Verilog, PERL.**
  - Developed Test Plan, Test Cases, Test Bench Architecture Block Diagram, translated Block diagram into code using Verilog and System Verilog; verified design using **QUESTASIM.**
  - Worked on Coverage Driven Random Verification using System Verilog.
  - Did post simulation testing using **PERL**.
  - Ran System Verilog Regression to check the functionality of the design.
  - Developed a UART Test Environment in System Verilog.

**May, 2013** **Design of HHO fuel cell for heat at home (Inspired by H2O Powered Car). – Out Of Course**
Built a circuit for electrolysis of H2O to produce H2 and O2, this circuit is a pulse charging circuit used for HHO fuel cell. **–with a local Gas Engineer Sal Cipolla.**

**Jan, 2013** **CA Technologies, Stony Brook, NY, USA.** **INTERN (8months)**
**Quality Assurance Team (Software Tester) – NIMSOFT PROJECT**
Developed widgets to be used in workflows, built using Signavio Editor. Also, developed independent test cases for continuous testing of "widgets", "dashboard" using Rest Client UI. – Programming Languages used: **PERL & C++**. –Manager Mr John Kane**.**

**Nov, 2011** **Unisoft Technologies, New Delhi, India** **Full Time (16months)**
**Software Developer – C++, HTML, XML, PHP.**

**Aug, 2010** Punjab University, India
**Bachelors of Electrical Engineering with honors** **GPA (3.6)**

## Projects:

**COMPUTER ARCHITECTURE:**

**Develop a dual-issue pipelined processor model (Instruction and Arithmetic Pipelining).**

- Implemented a dual-issue pipelined multi-stage RISC style architecture of SONY CELL SPU (Synergistic Processing Unit) in order to execute a set of 40 SPU instructions by successfully handling pipeline issues like structural and data hazards.
- An improved branch unit with RISC-style branch and jump operations is being designed adopting SIMD.
- Developed **Verilog** model of each pipelined multimedia unit such as storage, cache, processing and control units, using behavioral style coding and the final design is to be verified using a set of assembly level test programs. - **MODELSIM**

**DIGITAL:** **Design Verification and Test for VLSI circuits (NPTEL IIT)**
High Level Specification Algorithms, Front End Design Cycle and Automation Algorithms, Digital Testing and faults, built in Self-test (BIST), Combinational and Sequential Circuit Testing and Scan Chains.

**Designed a pipelined synchronous 4-bit adder with a goal to maximize clock frequency per average power consumption using HP 0.6u AMOS14TB process.**
The design and layout of the Adder done by considering various performance parameters like speed, power, and delay Verification/Extraction of the circuit in cadence custom IC design environment and performed simulations using Spectre Simulation tool.
– Tools Used: Virtuoso (**Cadence**), DRC/LVS (Cadence), NCSU library Design rules.

**VLSI (Physical & Logic Design) Design Automation: Partitioning (K-L Algo), Placement (Breuer's Algo) and Routing (Net-Merger Detailed Routing Algo).**
Coded using **C++ language** with goal to optimize the back-end design and tested the program using a set of benchmarks maintained by UCSD VLSI CAD Laboratory and Dragon Benchmarks.

**Performed explicit computations on image data in MATLAB.**
Geometric Transformation (Zoom In/Out); Spatial domain linear filtering, Frequency domain filtering using DFT and IDFT. – Tools: MATLAB

**ANALOG:** **Design of a 2-stage high gain high speed single ended operational amplifier in AMI 0.5 µm Technology.** – Tools Used: Virtuoso (Cadence), NCSU Library Design Rules, MATLAB.

**Design of a pipelined 8-bit ADC in AMI 0.5 µm Technology.**
Designed 1-bit MDAC with RA as a sub ADC to form an 8-bit pipelined ADC.

- Tools Used: Virtuoso (Cadence), NCSU Library Design Rules, MATLAB.

## Undergraduate Projects:

- Collision Avoidance Robot (microprocessor 8085).
- Solar Powered Automatic Railway Gate Control (8081 microcontroller).

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## Social Skills:

- IEEE Graduate Student member,
- Several awards for Technical Presentations both at University Level and State Level.