Low-Power Amplifier for Readout Interface of Semiconductor Scintillator

Xiao Yun, Student Member, IEEE, Milutin Stanačević, Member, IEEE, and Serge Luryi, Fellow, IEEE

Abstract—We present a design of readout system, comprising charge sensitive amplifier and pulse shaper, that directly interfaces semiconductor scintillator. Amplifier quantifies optical response of the large-area epitaxial photodiode, characterized by capacitance of 50 pF and dark current of 10 pA, that registers luminesce produced by scintillating semiconductor wafer in event of ionizing radiation event. Presented optimization procedure for biasing and sizing the input transistor of CSA directly relates the region of operation of the input transistor with constraints on power, area and event rate of the readout system. Experimental results of the amplifier implemented in 0.5 µm CMOS technology, verify gain of 71 mV/fC, with the linearity measured at 1.3%. For the parameters of photodiode, ENC is measured at 950 electrons with the time constant of pulse shaper 100 µs and the power consumption of 210 µW. The slope of ENC dependence on the input capacitance is measured at 18 e−/pF.

Index Terms—Radiation detection, scintillator, readout IC, charged sensitive amplifier, pulse shaper.

I. INTRODUCTION

Enhancement and deployment of radiological detection capabilities to prevent illicit use of nuclear devices or materials has been an increasingly important national security issue. Scintillating solid-state radiation detectors [1] register ionizing radiation by converting the energy of incident radiation into light measured by a coupled photo-detector. Due to inherent non-proportionality response and resulting poor resolution of dielectric scintillators [2], [3], the research of semiconductor scintillators could potentially bring a significant leap in energy resolution [4]. The challenge in implementing a semiconductor scintillator is how to make the material transmit its own infrared luminescence and two different approaches have been proposed for direct-gap semiconductors, like InP and GaAs. In the first, semiconductor is heavily doped with donor impurities, in order to introduce the Burstein shift between the emission and the absorption spectra [5]. The second approach is based on extremely high radiative efficiency of high-quality direct-gap semiconductor that leads to photon recycling [4]. Additional advantage of the semiconductor scintillator is the ability to integrate an epitaxial photodiode [6] on scintillator body for nearly perfect registration of the luminescence photons. Based on the Compton telescope technique [7], the three-dimensional array [4] of proposed radiation detectors, illustrated in Figure 1, provides accurate spectroscopic resolution for isotope discrimination and an accurate determination of the direction to the source at the same time. To measure the optical response of epitaxial photodiode, an application specific integrated circuit (ASIC) has to be integrated with the detector.

There has been a numerous examples of readout ASICs for radiation detection in literature [8]–[11], where circuit implementation and integration strongly depends on the detector and application. In the proposed semiconductor scintillator array, the size of the single pixel epitaxial photodiode is 1mm x 1mm. A large area of the photodiode leads to large sensor capacitance, measured at 50 pF [6]. A large detector capacitance leads to higher noise figures and potential instability in the amplifier design. However, the leakage current is rather low and is on the order of 10 pA. The main challenge in the design of the readout ASIC is minimization of the input noise in order to achieve the high sensitivity necessary to prevent false alarms caused by noise or legitimate radioactive materials. As proposed 3D integration calls for considerable volume with large number of pixels, a strict constraints are imposed on power consumption and size of the readout ASIC. Careful design of the readout system, especially the charge sensitive
amplifier (CSA), is required to properly compromise and optimize among noise, power, and area. Optimization procedures for sizing of the input transistor of CSA [12]–[14] have been concerned with accurate noise modeling and achieving unconstrained noise minimum. We will derive an optimization procedure that directly relates the region of operation of the input transistor with different constraints on the readout system using tractable models to describe transistor’s operation and noise. The optimization procedure will be applied in design of readout circuit to be integrated with the proposed scintillator and epitaxial diode into 3D array for radiation detection.

II. INPUT TRANSISTOR OPTIMIZATION

The readout system comprising charge sensitive amplifier and pulse shaper is adopted for the estimation of the theoretical noise floor in detection of an ionizing radiation event. Optimization of the input MOS transistor of CSA directly interfacing the photodiode is derived under assumption that the total noise contribution of the readout system is dominated by the input transistor. The sensitivity of the readout system is expressed through the equivalent noise charge (ENC) [16]. The ENC has three main components: white and flicker (1/f) series noise, originated in the input MOS transistor, and white parallel noise, due to the detector leakage current and feedback network [12]:

$$ENC_{ws}^2 = a_{ws} \frac{\gamma}{g_m} (C_p + C_g)^2 \frac{1}{\tau}$$  \hspace{1cm} (1)

$$ENC_{1/f}^2 = a_f K_F (C_p + C_g)^2$$  \hspace{1cm} (2)

$$ENC_{wp}^2 = a_{wp} I_{det} \tau$$  \hspace{1cm} (3)

where $a_{ws}$, $a_f$ and $a_{wp}$ are constants that depend on the type and order of the pulse shaper; $\gamma$ is the thermal noise coefficient that depends on the operation region of the transistor; $g_m$ and $C_g$ are the transconductance and gate capacitance of the transistor; $C_p$ is the load capacitance at the CSA input, which is the sum of the detector capacitance $C_d$, feedback capacitance $C_I$ and other parasitic capacitances resulting from the interconnect; $\tau$ is the time constant of the following shaper; $I_{det}$ is the detector leakage current and $K_F$ is the coefficient associated to the flicker noise of the input transistor.

As the transconductance and noise parameters of the transistor depend on the region of operation, the optimization procedure for sizing and biasing of the input transistor is formulated separately for strong and weak inversion region of operation. The transconductance of the transistor biased in strong inversion can be approximated as:

$$g_{m, strong} = \sqrt{2\mu C_{ox} I L}$$  \hspace{1cm} (4)

and in weak inversion as:

$$g_{m, weak} = \frac{I}{n U_T}$$  \hspace{1cm} (5)

where $n$ is the subthreshold slope coefficient, $U_T$ is the thermal voltage, $\mu$ is the mobility of the carriers in a specific process, $C_{ox}$ is the gate oxide capacitance per unit area, $I$, $W$ and $L$ are the biasing current, width, and length of the input transistor.

The flicker noise of MOS transistors may have two different origins [13], [15]. The $\delta N$ model assumes that the drain noise current is the result of fluctuation of charge carriers. The $\delta \mu$ model assumes that the fluctuation of charge carriers mobility generates the noise. Studies have shown that p-MOSFET might follow the $\delta N$ model when biased in weak inversion, and the $\delta \mu$ model when biased in strong inversion. Therefore, the 1/f flicker noise voltage spectral density $S_F$ can be expressed as:

$$S_{F, \delta N} = \left( \frac{q^2 n k T N_T}{2 \beta C_{ox}^2} \right) \frac{1}{2 \gamma L} \frac{1}{f}$$  \hspace{1cm} (6)

$$S_{F, \delta \mu} = \left( \frac{n q \alpha H}{2 \mu C_{ox}^2} \right) \frac{1}{\sqrt{W^3 L}} \sqrt{\frac{1}{f}}$$  \hspace{1cm} (7)

where $k$ is the Boltzmann constant, $T$ is the absolute temperature, $\alpha H$ is the Hooge constant, $N_T$ is the oxide/interface trap density per unit volume and energy at the quasi Fermi level, $\beta$ is the tunneling parameter of the traps. The $\delta \mu$ model predicts that the noise increases with the square root of biasing current $I$, while the $\delta N$ model predicts that the noise is independent of $I$.

A. Input transistor biased in strong inversion

Inserting (4) into (1), the spectral density model (7) of 1/f noise in (2), and using the approximate value of the gate capacitance $C_g = C_{ox} W L$, we obtain

$$ENC_{ws}^2 = \left( a_{ws} \frac{\gamma L}{q^2 \sqrt{2 \mu / n}} \right) \frac{(C_p + C_g)^2}{\sqrt{C_g}} \frac{1}{\sqrt{f}}$$  \hspace{1cm} (8)

$$ENC_{1/f}^2 = \left( a_f n q \alpha H L \right) \frac{(C_p + C_g)^2}{\sqrt{C_g}} \sqrt{\frac{1}{f}}$$  \hspace{1cm} (9)

The total ENC, when the input transistor is biased in strong inversion, can then be expressed as:

$$ENC_{tot, str}^2 = A_1 \frac{(C_p + C_g)^2}{\sqrt{C_g}} \frac{1}{\sqrt{f}} \tau + A_2 \frac{(C_p + C_g^2)}{\sqrt{C_g}} \sqrt{\frac{1}{f}} + A_3 \tau$$  \hspace{1cm} (10)

where $A_1$, $A_2$ and $A_3$ are constants, that follow from (8), (9) and (3). We assume that the length of input transistor is constant chosen to be slightly above the minimum value for the specific MOS technology. Thus, the total ENC is expressed in terms of three design variables: biasing current $I$, the gate capacitance of input transistor $C_g$ and shaping constant $\tau$.

An optimum value of $I$ exists as $ENC_{ws}$ decreases with $I$ while $ENC_{1/f}$ increases with $I$. An optimum $\tau$ exists as $ENC_{ws}$ and $ENC_{wp}$ share the same relation. For a fixed current $I$, if thermal and flicker noise are independently optimized, the minimum thermal noise is achieved for $C_g = 1/3 C_p$, while the minimum flicker noise is achieved for $C_g = 3 C_p$. 


1) Unconstraint optimization: If no limits are imposed to $I$ and $\tau$, an absolute minimum can be derived by calculating partial derivatives with respect to $I$, $C_g$ and $\tau$ of equation (10), and equating them to zero. The resulting optimal values are:

$$C_{g,opt} = C_p$$
$$I_{opt} = \frac{A_1 A_2 C_p}{16 A_2}$$
$$\tau_{opt} = \frac{A_1 A_2 C_p}{4 A_3}.$$ 

When the above optimum is feasible, $ENC_{ws} = ENC_{wp} = ENC_{1/f}$ and

$$\min[ENC_{tot, str}] = 3 \sqrt{16 A_1 A_2 A_3 C_p^2}$$

(12)

The above analysis is performed under the assumption that the input transistor is biased in strong inversion, therefore the optimal values for biasing current and gate capacitance from (12) have to satisfy the following condition [13]:

$$I > 5 I_S,$$

with

$$I_S = 2 n \mu C_{ox} U_T^2 \frac{W}{L}.$$

(14)

This leads to the upper limit on the size of transistor

$$C_g < \frac{10 I^2}{10 n \mu U_T^2}.$$ 

(15)

For the proposed detector with capacitance of 50 pF and leakage current of 10 pA, unconstraint optimization leads to a minimum ENC of 83 $e^-$ at a biasing current of 22 mA, which is significantly over the power consumption limit of the readout system. Optimal size of the input transistor for this case is 33.6 mm, while the optimal shaping constant is 11 $\mu$s.

2) Constraint optimization: The constraints on the optimization of the ENC originate from the rate of the radiation events, that presents the upper limit on $\tau$, total power consumption of the readout system, that limits the biasing current and the chip area, that limits the size of $C_g$. There is also an additional constraint related to the operation region of the input transistor, which is expressed in (15).

As derived in [13], when the biasing current is higher than $I_{opt}$, the suboptimum capacitive ratio tends toward $C_g/C_p = 3$ as the 1/f noise becomes dominant; when the biasing current is lower than $I_{opt}$, the suboptimum capacitive ratio moves to $C_g/C_p = 1/3$ as the thermal noise becomes dominant. If the biasing current is further lowered to a point that even $C_g/C_p = 1/3$ cannot keep the input transistor in strong inversion, the suboptimum is reached at $C_g/C_p = 1/3$.

If the shaping time constant is limited by the event rate, and must be shorter than $\tau_{opt}$, then the suboptimum biasing current is higher than $I_{opt}$ and the suboptimum capacitive ratio moves toward $C_g/C_p = 1/3$ since a shorter shaping time constant results in the larger thermal noise contribution.

B. Input transistor biased in weak inversion

The ENC for the case of the input transistor operating in weak inversion can be obtained by inserting the transconductance (5) in (1) and the $\delta N$ model (6) for 1/f noise in (2)

$$ENC_{ws}^2 = \frac{a_{ws}\gamma n k T}{I q} (C_p + C_g)^2 \frac{1}{\tau}$$

(16)

$$ENC_{1/f}^2 = a_f\left( \frac{q^2 n k T N_T}{2 \beta C_{ox}} \right) (C_p + C_g)^2$$

(17)

The total ENC can be expressed as:

$$ENC_{tot, weak}^2 = B_1 \frac{(C_p + C_g)^2}{I} \frac{1}{\tau} + B_2 \frac{(C_p + C_g)^2}{C_g} + B_3 \tau$$

(18)

where $B_1$, $B_2$ and $B_3$ are constants.

An optimum $\tau$ still exists. For a given $C_g$, $ENC_{tot, weak}$ decreases continuously as the biasing current $I$ is increased. If other parameters are fixed, the minimum thermal noise is achieved at the lowest $C_g$ while $C_g = C_p$ is the minimum for flicker noise.

1) Unconstraint optimization: In order to have the input transistor biased in weak inversion, the following condition applies [13]:

$$I < 0.01 I_S,$$

leading to

$$I < \frac{C_g n \mu U_T^2}{50 L^2}.$$ 

(20)

Therefore, the optimum $I$ is chosen as the largest current that keeps the input transistor in weak inversion.

$$I_{opt} = \frac{C_g n \mu U_T^2}{50 L^2}$$

(21)

The optimum $C_g$ and $\tau$ can be found by equating partial derivatives of (18) with zero, which gives the unconstraint optimum in weak inversion as:

$$C_{g,opt} = C_p$$
$$I_{opt} = \chi C_p$$
$$\tau_{opt} = 2 \frac{B_1}{B_3 \chi} C_p$$

(22)

where

$$\chi = \frac{n \mu U_T^2}{50 L^2}.$$ 

(23)

When the above optimum is feasible, the absolute minimum ENC in weak inversion is

$$\min[ENC_{tot, weak}^2] = 4 \sqrt{B_1 B_3 \chi C_p + 4 B_2 C_p}$$

(24)

With our specific sensor, the unconstraint optimization leads to the minimum ENC of 30e- at a biasing current of 44 mA, width of the input transistor at 33 mm and shaping constant of 124 $\mu$s. Therefore, the ENC is increased more than 4 times while the power consumption can be reduced by more than two orders of magnitude.
2) **Constraint optimization:** The conditions where each of the three design variables are limited are considered. If the biasing current \( I \) is fixed, the optimum \( \tau \) is calculated as

\[
\tau_{\text{subopt}1} = \frac{B_1}{B_3} (C_p + C_g). \tag{25}
\]

After inserting the optimum time constant into (18), it is observed that the white series noise, the optimum \( C_g \) is chosen as the smallest value to keep the transistor in weak inversion; for the flicker noise, the optimum \( C_g \) is at \( C_p \). Figure 2 shows a dependance of minimum ENC on biasing current.

If \( C_g \) is limited due to area constraint, the optimum biasing current has to be chosen as the largest value to keep the transistor in weak inversion, or \( I_{\text{subopt}2} = \chi C_g \). The optimum \( \tau \) can still be calculated as

\[
\tau_{\text{subopt}2} = \frac{B_1}{B_3} \chi \frac{C_p + C_g}{\sqrt{C_g}}. \tag{26}
\]

which gives the suboptimum ENC

\[
\text{ENC}_{\text{subopt}2} = 2 \frac{B_1 B_3}{\chi} \frac{C_p + C_g}{\sqrt{C_g}} + B_2 (C_p + C_g)^2/C_g. \tag{27}
\]

Figure 3 shows minimum ENC for different capacitive ratios of \( C_g \) and \( C_p \). We can notice that the minimum value of ENC worsens by 10% when the input transistor size is at 30% of its optimum value.

If the shaping time constant is fixed due to rate of ionizing radiation events, the same optimization procedure results in \( I_{\text{subopt}3} = \chi C_p \), \( C_g_{\text{subopt}3} = C_p \). The suboptimum ENC is calculated as

\[
\text{ENC}_{\text{subopt}3} = \frac{4B_1 C_p}{\chi} \frac{1}{\tau} + 4B_2 C_p + B_3 \tau. \tag{28}
\]

Figure 4 shows the minimum ENC as a function of time constant.

**C. Weak inversion and strong inversion comparison**

When absolute minimum noise is desired, the transistor would be biased in strong inversion. However, in circumstances where the biasing current of input transistor is limited due to power constraints, the optimal region of operation of the transistor depends on the power constraint. The optimum point also varies with different sensor parameters and noise requirements.

For our specific design, we have relatively flexible choices over time constant and input transistor size, while power consumption is our main concern. Figure 5 shows the minimum achievable ENC for the fixed biasing current if the input transistor operates in strong inversion or weak inversion. The biasing currents are limited to 100 \( \mu \)A, which is reasonable for most readout systems.

In strong inversion, ENC monotonically decreases as current increases. Since the input transistor cannot be large enough to be equal to \( C_p \), due to the relative small biasing current, the minimum ENC is always achieved when \( C_g \) is the largest value that keeps the input transistor in strong inversion. In weak inversion, a minimum ENC exists for \( C_g = C_p \), and the biasing current equals to the largest value that can keep the input transistor in weak inversion. From Figure 5, we can conclude that when biasing current is limited to 100 \( \mu \)A, the weak inversion is advantageous over strong inversion; when
the biasing current is higher, the strong inversion becomes preferred region of operation.

III. AMPLIFIER IMPLEMENTATION

The detailed circuit implementation of amplifier, comprising CSA and pulse shaper is outlined. The optimization technique proposed in Section II is applied for sizing of the input transistor.

A. Charge Sensitive Amplifier

Conventional architecture of CSA with high-gain amplifier and a small feedback capacitor for input charge integration is implemented as the first stage of amplification. In order to increase the overall gain provided by the input amplification stage, thus reducing the noise contribution of the subsequent pulse shaper, a two-stage cascaded charge-sensitive amplifier is implemented, as depicted in Figure 6. Pole-zero compensation network is formed by a parallel connection of $N_1$ replica of feedback network formed by capacitor $C_f$ and transistor $M_f$ and provides high linearity of the first-stage of CSA. A second CSA stage increases the overall gain by factor of $N_2$, leading to total gain of $N_1 \times N_2 = 100$ in the proposed implementation. To maintain high linearity of the CSA, the inverting points of both high-gain amplifiers are designed to be approximately equal. Choice of the feedback capacitance is influenced by the high detector capacitance and the feedback capacitances are set at $C_{f1} = C_{f2} = 500 \, \text{fF}$.

Figure 7 shows the folded-cascode implementation of high-gain amplifier in the first stage of CSA. p-MOSFET input transistor is chosen over n-MOSFET due to lower flicker noise. The width of the input transistor is 16.2 mm. DC gain of the folded-cascode amplifier is simulated at 94 dB. The leakage current of the detector is measured at 10 pA. The feedback transistor $M_f$ should be biased in the strong inversion in the saturation region of operation [17] to achieve lower noise. However, biasing of the feedback transistor $M_f$ in the strong inversion would require very long transistor due to low leakage current. Very long feedback transistor would lead to increased parasitic capacitance at the input node of CSA and as a consequence, $M_f$ is sized to operate in subthreshold region of operation at expense of increased input noise.

1) Noise contributions from other transistors: The additional noise contributions from $M_2$, $M_3$ and $M_5$ can be approximated as:

$$V_{n,add}^2 = (V_{n2}^2 g_{m2}^2 + V_{n5}^2 g_{m5}^2)/g_{m1}^2 + V_{n3}^2/C_{gd1} + C_{gs1} + C_p$$  \hspace{1cm} (29)$$

where $V_{n2}$, $V_{n5}$ and $V_{n3}$ are the input referred noise sources at the gate of $M_2$, $M_5$ and $M_3$ respectively. The input referred voltage noise from $M_2$ and $M_5$ is scaled by the transconductance of $M_1$. Because $M_2$ and $M_1$ have similar biasing current, and NMOS has at least one order of magnitude higher flicker noise coefficient than PMOS, the noise contribution from $M_2$ can not be neglected. To reduce the thermal noise from $M_2$, $g_{m2}$ has to be small, which leads to higher voltage drop for a fixed biasing current. To reduce the flicker noise from $M_2$, the transistor has to have large area while minimizing $g_{m2}$, which deteriorates stability of the amplifier, as discussed in the subsection III-A2. Therefore, it is also advantageous to bias $M_1$ in weak inversion and $M_2$ in strong inversion, so that the noise contribution from $M_2$ is contained. The noise from $M_3$ is coupled through $C_{gd1}$ to the input of the CSA. Since $M_1$ is normally very large, this component is not negligible. Considering the additional noise sources from (29),

![Fig. 6. Cascaded CSA implementation.](image)

![Fig. 7. Folded-cascode as high-gain amplifier in CSA.](image)

![Fig. 5. Minimum ENC as a function of fixed biasing current when the input transistor operates in weak and strong inversion.](image)
the optimization process has been modified, and the optimum is slightly different.

2) Stability analysis: As the large input transistor makes the non-dominant pole of voltage amplifier located at the cascode node closer to its dominant pole located at the gain node, the stability of CSA requires careful examination [18]. Assuming that the source follower is an ideal buffer and that the reset MOS transistor \( M_{f1} \) has a very large equivalent resistance \( R_f \), the open-loop circuit can be modeled as shown in Figure 8, where \( C_s = C_{gd1} + C_{gd2} + C_{gd3} + C_{gs} + C_f \) is the total capacitance at the folding node; \( r_o \) is the resistance of cascode of \( M_4 \) and \( M_5 \); and \( C_L \) is the capacitance at the CSA output. Thus, the loop gain can be derived as:

\[
A(s)\beta = \frac{V_{out}(s)}{I_{in}(s)} \beta = \frac{g_m(r_o||R_f)}{(\frac{s}{p_1} + 1)} \frac{(\frac{s}{p_2} + 1)}{(\frac{s}{p_3} + 1)}
\]

(30)

where zero and poles are located at

\[
\begin{align*}
    z_1 &= \frac{1}{R_fC_f} \\
    p_1 &= \frac{1}{R_f(C_f + C_p + C_g)} \\
    p_2 &= \frac{1}{(r_o|R_f)|(C_f + C_L)} \\
    p_3 &= \frac{g_m}{C_x}
\end{align*}
\]

(31)

\( p_1 \) is attributed to the feedback capacitor and the input capacitive load, \( p_2 \) and \( p_3 \) are the two poles associated to the voltage amplifier. The feed-forward zero comes from the \( RC \) feedback network. The unity-gain frequency \( f_u \) can be approximated as:

\[
f_u = \frac{g_mC_f}{(C_f + C_l)(C_p + C_f)}
\]

(32)

Since the first pole and zero are at relatively low frequency, their phase contribution can be approximately canceled. Therefore, the first non-dominant pole \( p_3 \) is critical and ultimately determines the phase margin of the loop. It is reasonable to assume that the CSA amplifier’s non-dominant pole is fixed, thus it is desired to place \( f_u \) far away from \( p_3 \). Smaller \( C_f \) makes the CSA more stable, however larger amplifier gain is required due to high \( C_p/C_f \) ratio. Thus, adding a compensation capacitive load \( C_L \) is the only feasible option. In our design, the values of \( C_L \) is 2 pF and achieved phase margin is over 70°. Though the added compensation capacitor slows down the circuit’s step response to over 3 \( \mu \)s, a time constant of 100 \( \mu \)s of following shaper makes the overall readout system unaffected.

Since the input capacitance of the second high-gain amplifier in Figure 6 is significantly smaller than for the first amplifier, the second amplifier is designed as a five-times scaled-down version of the first amplifier. Also, the additional compensation capacitor is not required for the second amplifier.

B. Pulse Shaper

The calculated optimum shaping time constant for the proposed amplifier is fairly large, 100 \( \mu \)s, as a consequence of high parasitic capacitance and low leakage current of the detector. Due to predicted low rate of ionizing radiation events, a long shaping time is affordable, without pile-up of events at the output of CSA. In order to achieve such long shaping time with the constraints of area and power, we have chosen R-lens filter that provides low-area and low-power shaper implementation [19]. The schematic of the two stages pulse shaper is shown in Figure 9(a). The ICON cell, shown in Figure 9(b), makes the equivalent resistance \( N \) times higher than the integrated physical resistance due to ratio of \( N \) in the current mirrors. The amplifiers in shaper are a scaled down version of the high-gain amplifier in CSA providing the same DC level to the amplifiers.

IV. RESULTS

The proposed readout system was implemented in 0.5\( \mu \)m CMOS technology. Figure 10 shows the micrograph of the single channel of the chip highlighting the functional blocks described in Sections III and III-B. Single channel measures 1.1 mm \( \times \) 0.4 mm. The characterization of the implemented preamplifier was conducted at 3.3 V supply voltage.
The fabricated preamplifier is characterized without sensor using interface printed circuit board. Chip-on-board technique was employed to wire-bond the die directly on board. A 1 pF capacitor that is connected externally to the input of the CSA enables controlled charge injection into the readout circuitry, as the current pulse at the input is generated by applying a known voltage step signal to capacitor. A dc current is injected into the input node of the CSA through 1 GΩ resistor and is controlled through on-board DAC. Different external capacitances at the input node, that model sensors capacitance, were used in characterization of the noise performance of the preamplifier.

Figure 11 shows a response of CSA for different voltage steps that correspond to the total input injected charge of 5k, 10k, and 20k electrons. The decay time of CSA is set in the order of ms, due to small leakage current of the detector and biasing of the feedback transistor in subthreshold region. Figure 12 shows measured output signal after the pulse shaper. A charge gain is measured at 71 mV/fC. The linearity of the CSA was measured at 0.4%, while the linearity of the amplifier, consisting of CSA and pulse shaper was measured at 1.3%. A plot of the output voltage of the amplifier as function of input charge is shown in Figure 13. The measure of sensitivity of the chip is ENC. Figure 14 shows the measured ENC for different values of input capacitance and the measured slope is 18 e−/pF. The power consumption of a single channel is measured at 210 µW.

V. CONCLUSION

The design and implementation of a low-noise, low-power amplifier for registration of the signal of semiconductor scintillator in case of ionizing radiation event is presented. For increased sensitivity of the readout circuitry limited by constraints of area, power and event rate, we have devised an optimization technique applied in the design of implemented CSA. The integration of the proposed readout amplifier and semiconductor scintillator in 3D array will provide isotope discrimination and an accurate determination of the direction of the source in applications like handheld radiation identifier that is suitable for patrol officers’ work in various entry ports.

VI. ACKNOWLEDGMENTS

The authors are grateful to Gianluigi De Geronimo (Brookhaven National Lab) for useful discussions and review of the paper. This work is supported by the Domestic Nuclear Detection Office (DNDO), Department of Homeland Security.
Fig. 14. Measured ENC as a function of the input capacitance.

REFERENCES


