Lab 12: BJT Common Emitter Amplifier

1. Objectives

Study and characterize BJT amplifier in Common Emitter (CE) configuration:

Determine the amplifier load line and find the DC operating point (Q-point);
Measure voltage gain, cut-off frequency and input impedance;
Appreciate the effect of shunt capacitor in emitter circuit on amplifier voltage gain and bandwidth.

2. Introduction

BJT Bias for CE amplifier

Figure 1 shows the so called "classic" bias for BJT. The bias circuit is just network of resistors. Power supply VCC and resistors R1 –R4 should set BJT to operate in the forward-active mode with required small signal parameters and well defined DC voltage level at the output. Figure 1 circuit uses R1-R4 and VCC values recommended for our lab experiments.

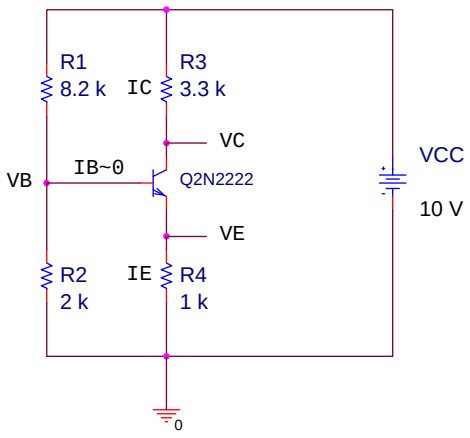

Figure 1

One can neglect the base current in preliminary estimation of the bias point[1]. Then:

Voltage divider R1-R2 defines the BJT base voltage VB: $$VB \approx VCC \cdot \frac{R1}{R1+R2},$$

VB establishes emitter voltage VE and emitter current IE: $$VE \approx VB - 0.7,$$

$$IE = \frac{VE}{R4} \approx IC$$

DC voltage level at the collector terminal VC is determined by R3:

$$VC = VCC - IC \cdot R3.$$

The value of the bias current IC should are used to calculate the small signal parameters g_m, r_π and r_0.

$$g_m = \frac{IC}{V_{th}}, r_\pi = \frac{\beta}{g_m}, r_O = \frac{V_A}{IC}$$

[1] Obviously more exact calculation can be performed using Thevenin theorem but in many cases it is not necessary.

Common Emitter Amplifier Operation

Figure 2 below shows the biased BJT in CE configuration. Observe the capacitors C1 – C3 that are to act as open circuits for DC and as short circuits for AC signals. The purpose of C1 capacitor is to make the DC operating point insensitive to the signal generator impedance. The bypass capacitor C2 is present to ground an emitter for AC signal and, hence, increase voltage gain of the amplifier. C3 is used to reinforce short circuit for AC signal across DC voltage source[2]. Resistor R5 serves two purposes: (a) attenuate signal from the generator not to saturate amplifier output and, hence, enable measuring of the high gains; (b) determine the gain stage input resistance R_{IN} by measuring voltage drop across R5. Voltage markers denote locations where the input (left marker, v_{in}) and output (right marker, v_{out}) signals are to be measured.

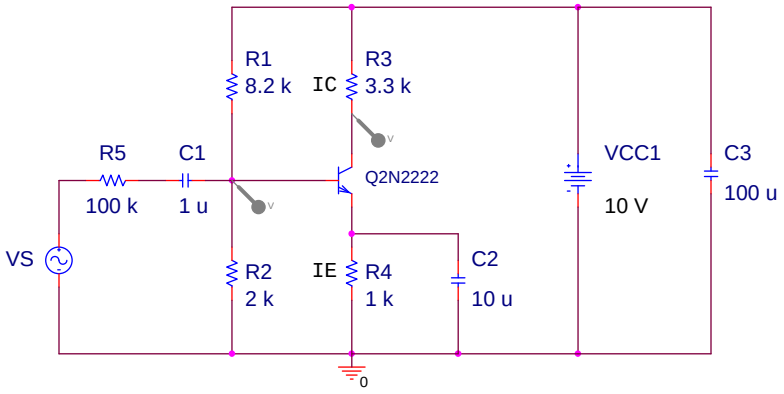

Figure 2

The circuit AC voltage gain is: $$A_V = \frac{v_{out}}{v_{in}} = \frac{-i_C \cdot R_3}{i_B \cdot r_\pi} = -\beta \cdot \frac{R_3}{r_\pi},$$

where i_C and i_B are signal (AC) collector and base currents, β – is common emitter current gain and the BJT's small signal output resistance r_O was neglected.

The circuit input resistance is: $$R_{in} = \frac{v_{in}}{i_{in}} = R_1 \parallel R_2 \parallel r_\pi .$$

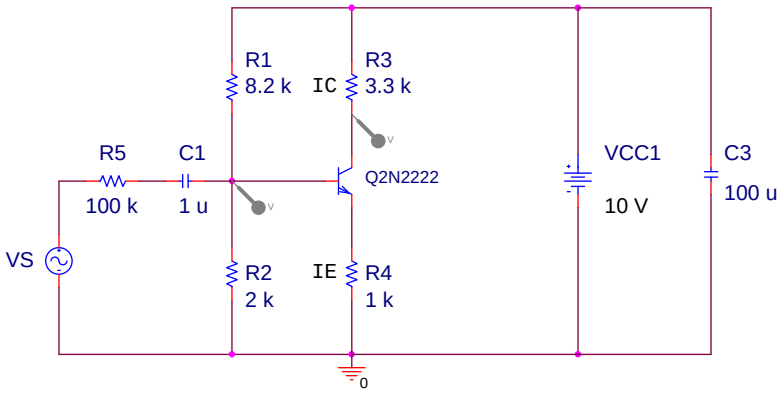

Figure 3

[2] Ideally any DC voltage source is short circuit for AC since voltage across DC voltage source can not be changed. In reality it is not always true so additional capacitors are to be used.

The stage in Figure 2 offers large voltage gain. However, the gain value varies with temperature T due to the dependences $\beta(T)$, $r_\pi(T)$. In contrast, the voltage gain of the circuit in Figure 3 depends only on resistances R3 and R4. In this circuit the bypass capacitor is removed and A_V decreases and R_{in} increases.

$$A_V = \frac{v_{out}}{v_{in}} = \frac{-i_C R_3}{i_B r_\pi + i_E R_4} \approx -\frac{R_3}{R_4},$$

$$R_{in} = \frac{v_{in}}{i_{in}} = R_1 \,||\, R_2 \,||\, \left(r_\pi + \beta \cdot R_4\right).$$

The BJT's parasitic capacitances between the emitter and base and between collector and base terminals lowers the voltage gain of CE amplifier at high frequencies. The latter capacitance (between base and collector) gives rise to so called Miller effect. Due to Miller effect the amplifiers with increased gain demonstrate decreased bandwidth. Gain-bandwidth product (GBW) in CE amplifies remains approximately constant.

In summary, the CE amplifiers are characterized by **(1) large current gain, (2) possibly large voltage gain BUT (3) relatively small bandwidth, (4) relatively small input impedance.** The voltage gain can be traded for wider bandwidth and higher input impedance (remove C2 and go from high gain to low gain but better bandwidth and input impedance).

3. Preliminary lab

Estimate the DC voltages and currents at the BJT terminals in the circuit in Figure 1. Sketch the DC and AC load lines for the circuit in Figure 2a. Estimate the maximum amplitude of undistorted output voltage.

Simulate in PSPICE the circuits in Figures 2 and 3. Obtain both the magnitude and phase responses in the frequency range from 10 Hz to 100 MHz.

4. Experiment

The experiments will be performed with a n-p-n BJT 2N2222A.

DC operating point

1. Assemble the circuit in Figure 1. Use DMM to measure the BJT DC operating point, which includes V_C and I_C. On Figure 4 draw DC load line and indicate the DC operating point (*bias point, Q-point are synonyms of DC operating point*).

Common Emitter Amplifier

2. Assemble the circuit in Figure 2. Apply a sin wave signal with amplitude of 1 V and frequency of 1 kHz. Use the oscilloscope; attach two probes to each side of R5. Measure both amplitudes and calculate R_{in}. Input voltage is measured directly at the right side of R5 while input current is calculated from voltage drop across R5. Note here that the signal from the right side of R5 will be very weak, so adjust oscilloscope sensitivity accordingly and manually measure the amplitude.

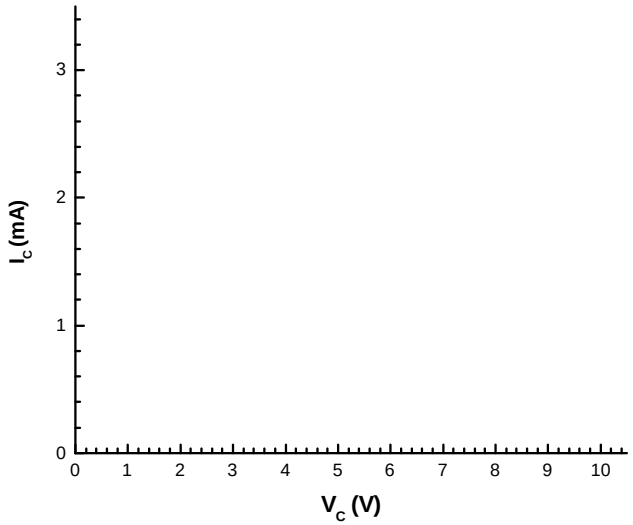

Figure 4

3. Attach two probes to the input and output of the amplifier as shown in Figure 2. Measure the frequency response. A frequency range from 10 kHz to 1MHz is recommended for this circuit. Take enough experimental points to resolve low and high frequency cutoffs. Present results in the Bode plot. Determine the mid-band voltage gain, -3dB cutoff frequencies[3] and the bandwidth.
4. Repeat steps 2 and 3 for the circuit in Figure 3. Observe the change of the mid-band gain and bandwidth.

Report

The report should include the lab goals, short description of the work, the experimental and simulated data presented in plots, the data analysis and comparison followed by conclusions. Please follow the steps in the experimental part and clearly present all the results of measurements.

[3] Low frequency cutoff point is determined by values of the coupling capacitors, C1- C3. High frequency cutoff is determined by transistor parasitic capacitances.