

Lab 9: CMOS inverter propagation delay.

1. OBJECTIVES

- Determine inverter input and output capacitances.
- Determine propagation delay of unloaded and loaded inverter.
- Observe an effect of power supply voltage.
- Observe an effect of switching activity on dissipated power.

2. INTRODUCTION

The dynamic of performance of a logic-circuit family is characterized by the propagation delay of its basic inverter. The inverter propagation delay (t_p) is defined as the average of the low-to-high (t_{PLH}) and the high-to-low (t_{PHL}) propagation delays:

$$t_p = \frac{t_{PLH} + t_{PHL}}{2}. \quad (1)$$

Propagation delays t_{PLH} and t_{PHL} are defined as the times required for output voltage to reach the middle between the low and high logic levels, i.e. 50 % of V_{DD} in our case of CMOS logic. Figure 1a illustrates the definition of the propagation delays.

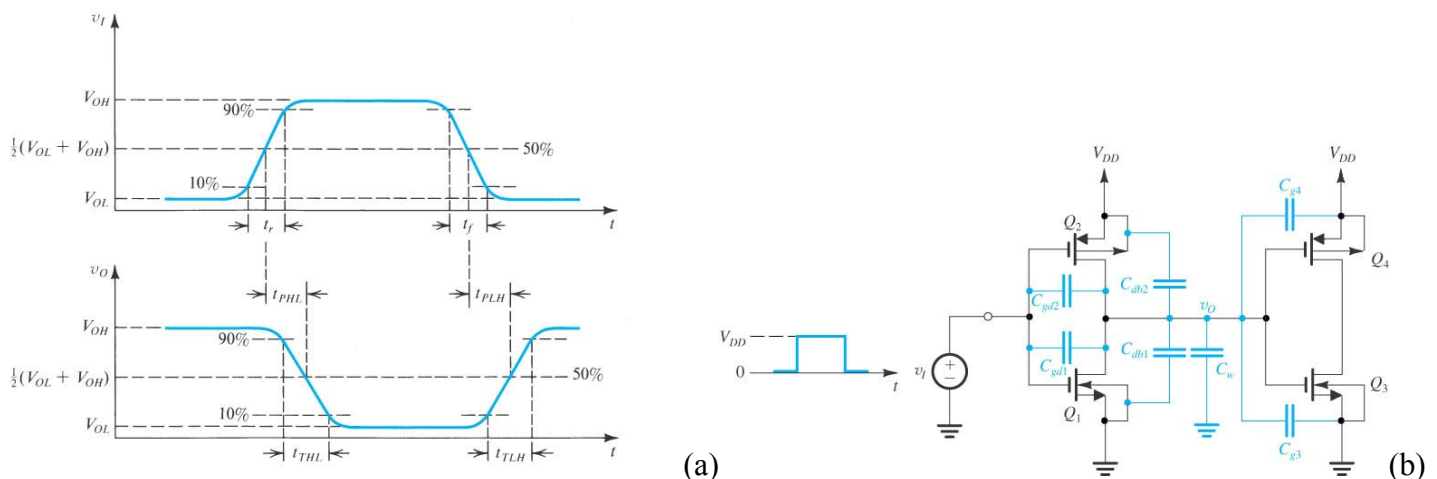


Figure 1. (a) Definition of propagation delays of logic inverter; (b) Circuit illustrating capacitances determining the inverter propagation delay.

The propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the capacitances present in the logic circuit. Figure 1b shows the circuit for analysis of the propagation delay of the inverter under condition that it is driving an identical inverter. To make the analysis tractable it is convenient to replace capacitances attached to the output node of primary inverter (Q_1 - Q_2 in Figure 1b) with equivalent capacitances between output node and ground. This is considerable simplification but individual consideration of every capacitor including nonlinear capacitances in the MOS transistor model makes a manual analysis virtually impossible. Hence, for our purposes we adopt this simplified model that is adequate for qualitative

analysis and allows making estimation of CMOS inverter propagation delay. Figure 2 shows the “inverter driving inverter circuit” where all capacitors are lumped together to form three equivalent capacitors connected between output and ground of the primary inverter.

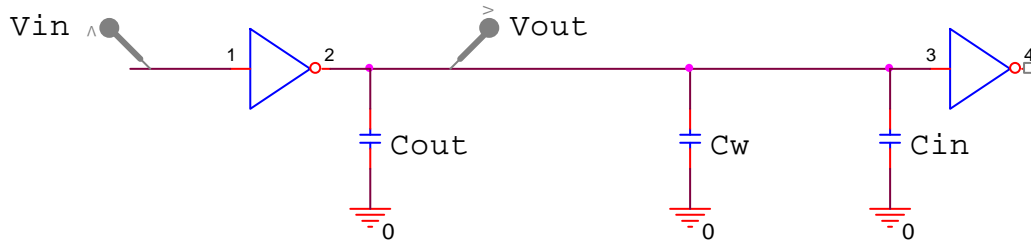


Figure 2.

The total load capacitance of the primary inverter is:

$$C_L = C_{OUT} + C_W + C_{IN}, \quad (2)$$

Where:

$$C_{OUT} = 2 \cdot (C_{gd1} + C_{gd2}) + C_{db1} + C_{db2}, \quad (3)$$

$$C_{IN} = C_{g3} + C_{g4}, \quad (4)$$

and C_W – wiring or any other extra load capacitance.

The physical meaning of each of the transistor capacitances was discussed during lecture time.

The propagation delay of the CMOS inverter that is loaded only with its own output capacitance C_{OUT} is called intrinsic delay:

$$t_{p0} = \frac{t_{PLH0} + t_{PHL0}}{2}. \quad (5)$$

In the simplified analysis the NMOS and PMOS transistors can be replaced by equivalent resistances R_{EQN} and R_{EQP} when charging and discharging the C_{OUT} resulting into (another significant simplification):

$$t_{PLH0} \approx 0.69 \cdot R_{EQP} \cdot C_{OUT}, \quad (6)$$

$$t_{PHL0} \approx 0.69 \cdot R_{EQN} \cdot C_{OUT}. \quad (7)$$

Thus it is assumed that PMOS acts as a R_{EQP} when C_{OUT} is charged to V_{DD} when output is switched from low-to-high and NMOS acts as a R_{EQN} when C_{OUT} is discharged when output is switched from high-to-low.

Propagation delay of the loaded inverter can be expressed through intrinsic delay:

$$t_p = t_{p0} \cdot \left(1 + \frac{C_{IN} + C_W}{C_{OUT}} \right). \quad (8)$$

The values of the equivalent resistances and even C_L can depend on V_{DD} thus the propagation delay is affected by power supply voltage (being smaller for higher V_{DD}). It should be noted, however, that this dependence of the propagation delay on power supply voltage is less pronounced in MOSFETs with short channels where drain current saturation is achieved due to velocity saturation rather than due to channel pinch-off at drain.

Measurement of the C_{IN} and C_{OUT} can be performed using the following approaches:

1. Measurement of C_{OUT} .

Once the propagation delay of an unloaded inverter is known (intrinsic propagation delay) one can determine the C_{OUT} from equation (8) by measuring propagation delay of the loaded inverter (Figure 3). The load capacitance should be dominant, i.e. $C_W \gg C_{OUT}$, and must be known with high precision.

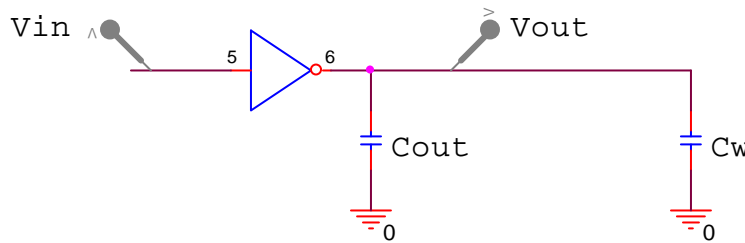


Figure 3.

2. Measurement of C_{IN} .

Input capacitance of the inverter can be determined by driving it with square wave input from low output impedance function generator connected in series with known resistance (Figure 4). Clearly, the R_S is supposed to be measured precisely. Input capacitance of an inverter creates a series RC circuit with the source resistance. When V_S switches from low-to-high, V_{in} will exponentially rise from zero to V_{DD} :

$$V_{in} = V_{DD} \cdot \left(1 - \exp\left(-\frac{t}{R_S \cdot C_{IN}}\right) \right) \quad (9)$$

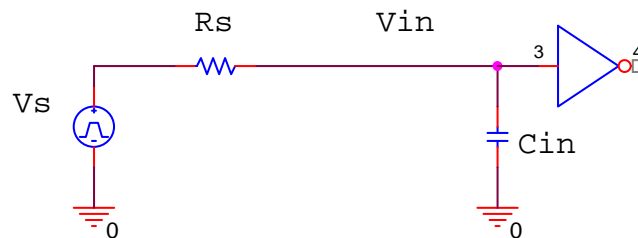


Figure 4.

Power dissipation

Dynamic power dissipation of the digital logic circuit depends on power supply voltage V_{DD} , on circuit capacitances (for CMOS inverter studied - C_L) and on switching activity f . Static and direct path power dissipations are often smaller than P_{dyn} and can be neglected in the basic analysis. P_{dyn} is given by:

$$P_{dyn} = C_L \cdot V_{DD}^2 \cdot f \quad (10)$$

In this lab we will observe the dependence of the average dissipated power in the unloaded and loaded inverter as a function of the switching frequency.

3. PRELIMINARY LAB

3.1. What frequency of the input square wave signal (50 % duty cycle) would you select to measure (by an oscilloscope) 10 ns low-to-high and high-to-low propagation delays of the inverter. Selected frequency should allow for simultaneous observation of low-to-high and high-to-low transition on oscilloscope screen.

3.2. For circuit in Figure 4. Assume that $C_{in} = 10$ pF and $R_s = 100$ k Ω . What frequency of the square wave input would be adequate to measure the RC time constant of the circuit based on exponential charging or discharging of C_{in} ?

3.3. Assume inverter with intrinsic propagation delay of 10 ns. Assume $C_{in} = 10$ pF, $C_{out} = 10$ pF (Figure 2). For $C_W = 0, 10$ and 100 pF find a propagation delay of the “inverter driving inverter”. Determine the maximum switching frequency of the circuit for each C_L .

3.4. Find the dynamic power dissipation for the inverters from 3.3 operated at their maximum switching frequencies. Assume $V_{DD} = 5$ V. What is average value of the DC current flowing from power supply to ground in corresponding CMOS inverter circuits?

3.5. Compare the dynamic power dissipation for the inverters from 3.3 operated at the same frequency - maximum switching frequency of the slowest inverter. Assume $V_{DD} = 5$ V. What is average value of the DC current flowing from power supply to ground in corresponding CMOS inverter circuits?

4. EXPERIMENT.

We will use CD4007 CMOS array to construct inverters for this lab. MOSFETs in CD4007 are not matched; hence, expect asymmetric inverter voltage transfer characteristics and different equivalent resistances for NMOS and PMOS (see datasheet).

4.1. Construct two separate CMOS inverters using single CD4007 chip. Use $V_{DD} = 5$ V. Determine an intrinsic propagation delay for each inverter. Namely: (1) apply 0-to-5 square wave to input; (2) visualize both input and output waveforms on oscilloscope screen; (3) select frequency of input signal to see clearly low-to-high and high-to-low transition at the output (1 to 5 MHz); (4) record input and output waveforms; (5) measure t_{PLH0} and t_{PHL0} and calculate t_{p0} according to (5) for each inverter. Estimate the maximum switching frequency for the unloaded inverters. Comment on matching between NMOS and PMOS.

4.2. Construct circuit from Figure 3 using one of the inverters. Measure propagation delay of the loaded inverter for $C_L = 100$ pF and $C_L = 1$ nF. Be sure to measure actual values of capacitances. Beware that input frequency will need to be reduced substantially for this measurements. Calculate C_{OUT} assuming that C_L dominates the propagation delay. Estimate the maximum switching frequency of the loaded inverter.

4.3. Construct circuit from Figure 4 using another inverter. Use $R_s \approx 100$ k Ω . Be sure to measure actual values of resistance. Select input frequency so the transition time of V_{in} for charging and discharging C_{IN} can be observed on oscilloscope screen. Determine C_{IN} using equation (9).

4.4. Construct circuit from Figure 2 using inverter from 4.2 as a primary and the one from 4.3 as a secondary. Do not connect C_W . Measure propagation delay. Comment on relative roles of C_{IN} and C_{OUT} in determining a propagation delay of the “inverter driving inverter” circuit.

4.5. Repeat 4.1 for one of the inverters using $V_{DD} = 2$ V. Be sure to change input square wave to 0-to-2 V. Explain the change in intrinsic propagation delay.

4.6. Change V_{DD} back to 5 V and input square wave to 0-to-5 V. Measure average (DC) current flowing from power supply (V_{DD}) to ground when varying the input frequency from 1 kHz to 10 MHz. Determine the power dissipated by inverter at each frequency. Repeat for inverter loaded with $C_L = 100$ pF. Compare the measured power dissipation with the prediction of equation (10).

4. REPORT

The report should include the lab goals, short description of the work, the experimental and simulated data presented in plots, the data analysis and comparison followed by conclusions. Please follow the steps in the experimental part and clearly present all the results of measurements. Be creative; try to find something interesting to comment on.