Lab 2: Common Source Amplifier.

1. OBJECTIVES

Study and characterize Common Source amplifier:

Bias CS amp using MOSFET current mirror;
Measure gain of CS amp with resistive load;
Measure gain of CS with active load.

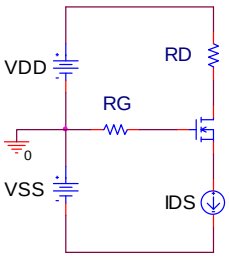
2. INTRODUCTION

2.1. CS amplifier bias.

Common Source (CS) configuration of single stage MOSFET amplifier can offer substantial voltage gain in combination with large input impedance. When operated at relatively low frequencies, the CS amplifier can be modeled replacing the MOSFET with small signal equivalent circuit that uses only two parameters. Namely, gate transconductance g_m and output resistance r_0. Both of these parameters are dependent on MOSFET bias, i.e. DC drain current set by bias circuit. Equations (1) and (2) can be applied to estimate MOSFET gate transconductance and output resistance within framework of LEVEL 1 model.

Gate transconductance:
$$g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)\Bigg|_{V_{DS}} \approx \frac{W}{L}\cdot\kappa_n\cdot\left[V_{GS}-V_T(V_{SB})\right] = \sqrt{2\cdot\frac{W}{L}\cdot\kappa_n\cdot I_{DS}} \qquad (1),$$

Output resistance:
$$r_O = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1}\Bigg|_{V_{GS}} = \left(\lambda\cdot\frac{W}{L}\cdot\kappa_n\cdot\frac{\left[V_{GS}-V_T(V_{SB})\right]^2}{2}\right)^{-1} \approx \frac{V_A}{I_{DS}\big|_{V_{DS}\to 0}} \qquad (2).$$



The maximum value of the open circuit voltage gain that can be obtained from CS amplifier is thus also dependent on bias:
$$A_{VO} = -g_m\cdot r_O \propto 1/\sqrt{I_{DS}} \qquad (3).$$

Equation (3) suggests that it could be advantages to reduce bias current. However, if the drain resistance (RD in figure) is smaller than r_0 then the voltage gain will increase with bias thanks to transconductance increase. Open circuit voltage gain becomes:
$$A_{VO} \approx -g_m\cdot R_D \propto \sqrt{I_{DS}} \qquad (4).$$

As long as $R_D << r_0$, the increase of R_D will lead to higher gain. However, the maximum value of R_D that could be afforded is often restricted by DC value of drain current I_{DS}. The reason is that voltage drop across R_D consumes part of the power supply voltage. DC voltage at drain of NMOS will be:
$$V_D = V_{DD} - I_{DS}\cdot R_D \qquad (5).$$

This voltage has to be sufficient not to drive NMOS into triode region. For the specific case shown in basic circuit shown in figure, i.e. when gate DC voltage is equal to zero, V_D must satisfy:
$$V_D > -V_T \qquad (6).$$

The value of V_D equal to $-V_T$ corresponds to boundary between saturation and triode regions. Thus the

maximum signal voltage swing at the output is from V_{DD} to $-V_T$. Hence the value of the bias current I_{DS} will determine maximum positive (+ΔVmax) and negative (-ΔVmax) output voltage swings:

$$\left|+\Delta V_{max}\right| = V_{DD} - V_D = V_{DD} - \left(V_{DD} - I_{DS}\cdot R_D\right) = I_{DS}\cdot R_D$$
$$\left|-\Delta V_{max}\right| = V_D - \left(-V_T\right) = V_{DD} - I_{DS}\cdot R_D + V_T \qquad (7).$$

Of course, the real life circuits can be more involved than the simplified example shown in the figure above and additional voltage drops has to be taken into account (see, for instance, an active load case discussed later or case of extra DC bias on gate). However, the logic for estimation of signal swing of linear amplifier remains essentially the same – if MOSFET was in saturation with no signal, the signal should not drive it into nonsaturation.

In our experiments, MOSFET basic current mirror will be used to bias CS amplifier. The pin-outs of two MOSFET array chips that we are using are given below. Two NMOS FETS from CD4007 array will be used to construct basic current mirror. CS amplifier will be build based on ALD1105 NMOS transistor. Active load will be realized using two ALD1105 PMOS transistors.

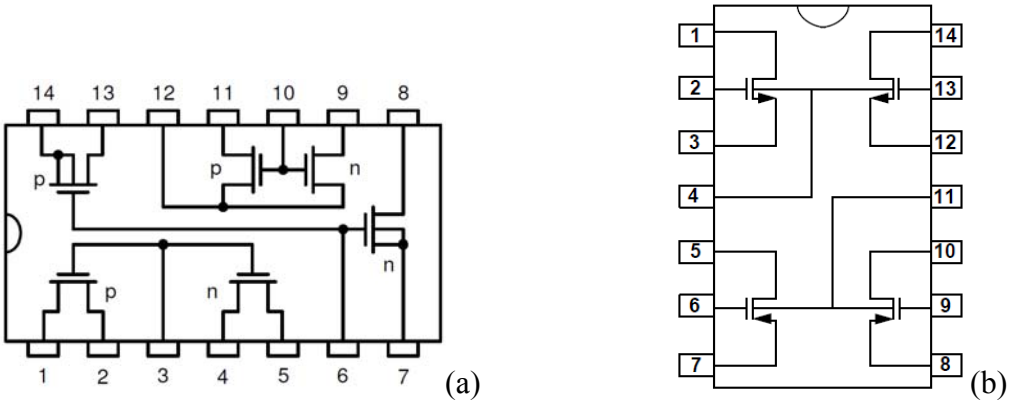


Figure 1. Pin-out of (a) CD4007 and (b) ALD1105 MOSFET array chips.

Current mirror can be constructed using (gate-3, source-4, drain-5) and (gate-6, source/body-7, drain-8) NMOS transistors from CD4007 array as M1 and M2, respectively, in circuit shown in Figure 2. For a given power supply voltage the value of ID1 can be set by adjusting the potentiometer R. The current ID1 is to be mirrored to ID2 but, as we have learned in lab 1, will depend on VDD2 due to finite small signal output resistance of M2.

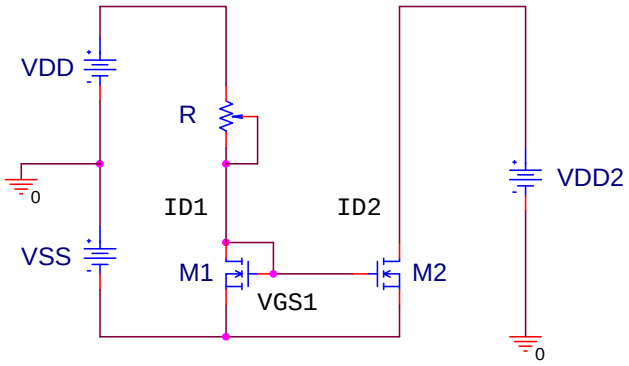


Figure 2.

2.2. CS amplifier with resistive load.

Consider the circuit in Figure3. M3 NMOS can be made out of (1,2,3,4) pins of ALD1105. Here the input signal is applied directly to gate of M3. The output signal is taken from drain of M3 with respect to ground. R_D serves as a resistive load, i.e. determines the transistor gain and limits output swing. Bypass capacitor C_S is required to obtain gain otherwise the current through M3 would not change (well, almost would not change) and no (actually, almost no) output will be produced in response to the input.

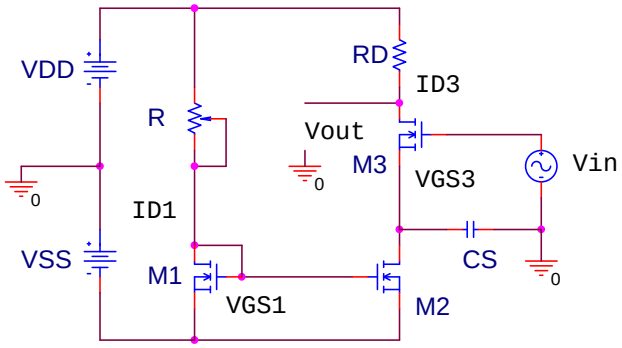


Figure 3

To do a DC bias analysis one can ground the gate of M3 and ignore C_S. Clearly, DC voltage at the drain of M3 should be above $-V_T$ of M3, i.e. $-V_{TM3}$. Pay attention to the fact that we connected the bulk and source terminals of M3 together. This is a luxury the discrete element designer can afford and integrated circuit (IC) designer cannot. Strictly speaking, we should have connected the bulk of M3 to –VSS to mimic IC design. Then, the V_{TM3} would be increased due to body effect. Let us simplify things for now and keep M3 "free of body effect".

In Figure 3 circuit, the drain-to-source voltage of M2 should be above $V_{GS1} - V_{TM2}$ not to drive M2 into nonsaturation. Also, source of M3 should be at voltage smaller than $-V_{TM3}$ to have M3 open. Value of R_D is selected based on desired gain and output voltage swing.

2.3. CS amplifier with active load.

Figure 4 shows the CS amplifier loaded with current source. This current source is made of basic PMOS current mirror. Both PMOS transistors from ALD1105 are used to construct this active load.

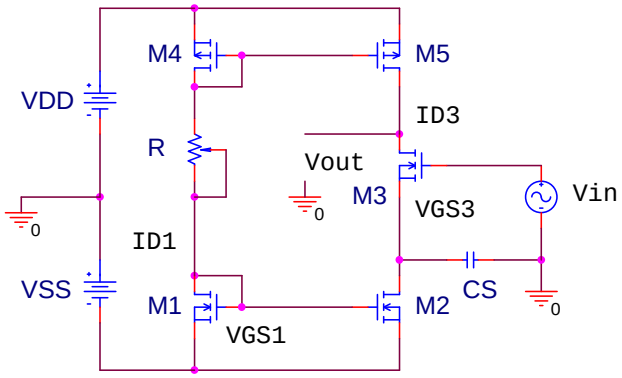


Figure 4.

The output impedance for the PMOS current mirror is r_0 of M5 and this r_{0M5} serves as a load in small signal equivalent circuit for gain calculations. The gain of the CS amplifier with active load becomes:

$$A_{VO} = -g_{mM3} \cdot (r_{OM3} \parallel r_{OM5}) \qquad (8).$$

This value is often much larger than gain of the amplifier with resistive load. Clearly, the value of R has to be adjusted to keep M2 bias the same as in Figure 3 circuit since extra voltage will drop across M4. Also, M5 will restrict maximum positive voltage swing at the output.

3. PRELIMINARY LAB

3.1. For the circuit in Figure 2 assume $V_{DD} = V_{SS} = 5$ V. For both M1 and M2 assume $V_T = 1$ V and $W/L*k_n = 0.8$ mA/V^2. Estimate R required to have drain current ID1 equal to 250 μA. Find the corresponding value of gate-to-source voltage of M1 and M2. Determine the minimum value of VDD2 for M2 to remain in saturation.

3.2. For the circuit in Figure 3 assume that M3 is biased with 250 μA. Assume $V_{DD} = V_{SS} = 5$ V. For M3 assume $V_T = 0.7$ V. Estimate the maximum value of RD to have negative output voltage swing of 1 V.

3.3. For the circuit in Figure 4 assume M1 parameters from 3.1, $V_{DD} = V_{SS} = 5$ V. For M4 assume $V_T = -0.7$ V. Estimate the maximum value of R to have ID1 = 250 μA. Ignore overdrive voltage for M4 in this rough estimation.

4. EXPERIMENT

4.1. Build the circuit shown in Figure 2 using VDD = VDD2 = VSS = 5 V. Select 50 kΩ potentiometer and adjust it to obtain ID1 = 250 μA. Measure VGS1 and ID2. Measure the actual value of R.

Explain difference between ID1 and ID2.Compare measured VGS1 and R with the results of your prelab calculations.

4.2. Augment circuit from Figure 2 with RD and NMOS (ALD1105) to obtain circuit from Figure 3. At this point do not use CS and do not connect any signal source, i.e. ground gate of M3. Select RD according to your prelab calculation (it is in the range from 10 to 20 kΩ). Adjust potentiometer R to obtain DC drain currents of M3 equal to 200, 250 and 300 μA. Measure corresponding values of V_{GS} for M3.

Estimate gate transconductance of M3 near 250 μA bias. Calculate value of the open circuit voltage gain.

4.3. Adjust potentiometer R to have 250 μA bias for M3. Apply sinusoidal input signal with 100 mW amplitude and 1 kHz frequency. Obtain both input and output signals on oscilloscope screen. Measure their peak-to-peak values and relative phase. Augment circuit with CS ~ 1 μF and repeat the measurements. Increase the amplitude of the input sinusoidal until distortions start to appear in output waveform. Measure the maximum amplitude of the undistorted output signal.

Present the measurement results in the form of table. Find the value of the open circuit voltage gain. Compare with calculation results from 4.2. Explain effect of CS on voltage gain. Compare measured amplitude of the maximum undistorted output signal with estimations from prelab.

4.4. Augment the circuit from Figure 3 with PMOS transistors (ALD1105) to obtain the circuit from Figure 4 (of course, remove RD). Adjust R to have 250 μA bias for M3. Measure V_{GS} for M4. Reduce amplitude of the input signal (you might want to use voltage divider) to obtain undistorted output waveform. Measure the open circuit voltage gain of the amplifier with active load.

Explain the difference in voltage gains in CS amplifiers with resistive and active loads. Sketch the distorted and not distorted output waveforms. You can use oscilloscope memory function to take waveform data.

5. REPORT

The report should include the lab goals, short description of the work, the experimental and simulated data presented in plots, the data analysis and comparison followed by conclusions. Please follow the steps in the experimental part and clearly present all the results of measurements. Be creative; try to find something interesting to comment on.