

Lab 8: CMOS inverter.

1. OBJECTIVES

- Understand CMOS inverter static voltage transfer characteristics.
- Characterize switching threshold, noise margins and on-state resistance.
- Study effect of power supply voltage on voltage transfer characteristics.

2. INTRODUCTION

The inverter is a basic building block of all digital designs. The behavior of more complex digital logic gates (NAND, NOR, XOR) as well as adders, multipliers and even microprocessors can be derived by extrapolating the results obtained for inverters. In this laboratory experiment we will characterize the static behavior of CMOS inverter (Figure 1a). An operation of this circuit can be understood using simple switch model of MOS transistors (Figure 1b). In this simplistic model the transistors are just switches with infinite off-state and finite on-state resistances (r_{DSP} and r_{DSN}). The transition between off- and on-states occurs when appropriate voltage is applied to gate. For instance, NMOS transistor in Figure 1 would go from off- to on-state when gate voltage becomes more positive than NMOS threshold (V_{TN}). The same logic is applicable to PMOS transistor, i.e. gate voltage that is more negative than PMOS threshold (V_{TP}) would switch the PMOS on. Thus, when the input voltage is low, the NMOS in Figure 1 is off and no current can flow between its gate and source (well, almost no current). At the same time, low input voltage means the whole V_{DD} applied to gate of PMOS, hence, PMOS is on and output is tied to V_{DD} through channel of this pull-up PMOS transistor. Once input is at V_{DD} , PMOS is off and NMOS is on. Now, NMOS acts as a pull-down transistor connecting output to ground. So the circuit performs as an inverter: low input causes high output and vice versa.

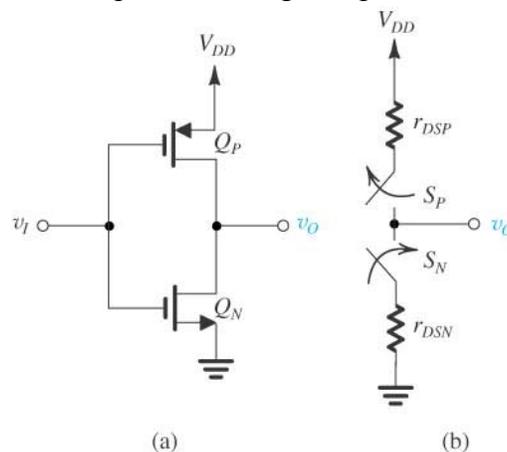


Figure 1. Q_P - PMOS and Q_N – NMOS. Bulk contacts (not shown) of NMOS and PMOS are connected, respectively, to the most negative and to the most positive voltages available in the circuit.

Figure 1 circuit would operate as an inverter even if power supply voltage is below transistor thresholds. The reason is nonzero under threshold conduction of MOSFETs. MOSFET operating below threshold is operating in so called weak inversion regime (low charge carrier concentration in channel). Weak inversion regime is good for low power applications but limits circuit speed.

Figure 2 shows the generic static voltage transfer characteristics of inverter and illustrates the definition of the critical points. Namely: output high (V_{OH}) and low (V_{OL}) levels, input high (V_{IH}) and low (V_{IL}) levels, and switching threshold V_M .

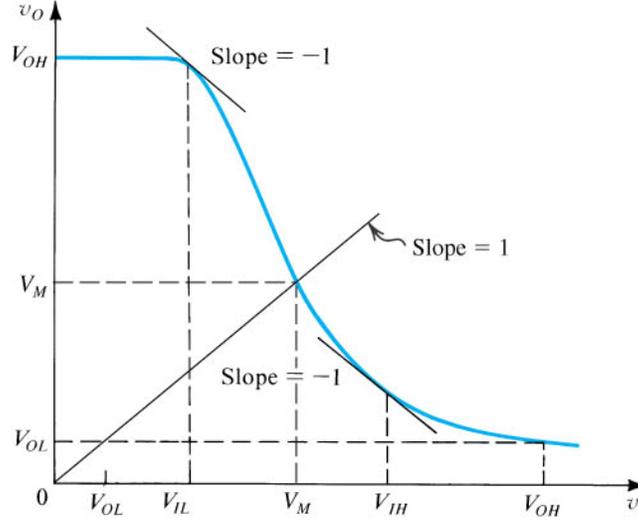


Figure 2.

Noise margins determine the range for input signal to be considered low or high. For $V_{OL} = 0$ and $V_{OH} = V_{DD}$:

$$NM_H = V_{DD} - V_{IH} \text{ and } NM_L = V_{IL}, \quad (1)$$

where V_{IH} and V_{IL} , i.e. operational points of the inverted where $\frac{dV_{OUT}}{dV_{IN}} = -1$, are:

$$V_{IH} = V_M - \frac{V_M}{g} \text{ and } V_{IL} = V_M + \frac{V_{DD} - V_M}{g}. \quad (2)$$

In equation 2 the actual voltage transfer characteristics is replaced with its piece-wise model with slope at switching threshold characterized by g – gain at switching threshold:

$$g = -\frac{V_{DD}}{V_{IH} - V_{IL}}. \quad (3)$$

The values of g and V_M are determined by technology parameters and power supply voltage, i.e. MOSFET operation mode. For matched transistors, i.e. for $V_{TN} \approx -V_{TP}$ and $\left(\frac{W}{L} \cdot k'\right)_N \approx \left(\frac{W}{L} \cdot k'\right)_P$, switching threshold is about $V_{DD}/2$. Any transistor mismatch would lead to shift of V_M and, hence, change of noise margins. Fortunately, the dependence of V_M on transistor parameter variation is weak for CMOS inverter.

The finite g is caused by finite output impedances of NMOS and PMOS, hence it is dependent on power supply voltage. Finally, static on-state resistances of the NMOS and PMOS transistors can be estimated as:

$$r_{DSN} = \left[\left(\frac{W}{L} \cdot k' \right)_N \cdot (V_{DD} - V_{TN}) \right]^{-1} \text{ and } r_{DSP} = \left[\left(\frac{W}{L} \cdot k' \right)_P \cdot (V_{DD} - |V_{TP}|) \right]^{-1}. \quad (4)$$

3. PRELIMINARY LAB

3.1. Assume that NMOS and PMOS transistors both have the same gate oxide capacitance per unit area but mobility of holes is about 3 times lower than that of electrons. Assume that $V_{TN} = -V_{TP} \approx 0.5$ V. Find the switching threshold of the CMOS inverter made of these NMOS and PMOS transistors for $V_{DD} = 2.5$ V. Assume that both transistors have the same aspect ratio, i.e. $(W/L)_N = (W/L)_P$.

3.2. Assume NMOS and PMOS transistors from 3.1. Assume that channel length is fixed by technology and the same for both FETs. Find the ratio of channel widths of PMOS and NMOS transistor to result into symmetric CMOS inverter voltage transfer characteristics, i.e. $V_M = V_{DD}/2$.

3.3. Explain dependence of the CMOS inverter voltage transfer characteristics on power supply voltage V_{DD} .

3.4. CMOS inverter is made of NMOS with on-state resistance of 500Ω and PMOS with on-state resistance of 1500Ω at $V_{DD} = 2.5$ V. Input is grounded. Find the output voltage when inverter is loaded with (1) open circuit; (2) $10 \text{ k}\Omega$, (3) 1500Ω and (4) 500Ω .

4. EXPERIMENT.

We will use ALD1105 CMOS array to construct inverters for this lab. NMOS and PMOS FETs in ALD1105 are not matched, namely, $V_{TN} \approx -V_{TP}$, but NMOS and PMOS drive different currents under the same voltage bias (see datasheet). We can adjust that to some extent by building inverters using parallel connection of either NMOS or PMOS transistors.

Remember that parallel connection of two identical MOS transistors (connect together gate, source and drain terminals of two MOSFETs) is roughly equivalent to having MOSFET with twice the channel width.

4.1. Assemble CMOS inverter using two NMOS connected in parallel and single PMOS. Apply $V_{DD} = 2.5$ V. Perform point by point measurements of the voltage transfer characteristics by varying DC input voltage V_{IN} from zero to V_{DD} and measuring DC value of V_{OUT} . Simultaneously, keep track of the DC drain current flowing through NMOS and PMOS. Plot voltage transfer characteristics and dependence of DC current on V_{IN} . Estimate V_M and noise margins. Explain observed dependence of DC current on V_{IN} .

4.2. Repeat 4.1 procedure for inverter made of single NMOS and two parallel connected PMOS FETs. Compare with 4.1. Comment on observed differences. Which inverter has the most symmetric voltage transfer characteristics? Explain the reason for this.

4.3. Select an inverter (between 4.1 and 4.2 versions) with the most symmetric voltage transfer characteristics. Apply saw-tooth wave input (ramp) waveform: 1 kHz, from zero to V_{DD} . You would need to use offset of $V_{DD}/2$. Obtain both input and output waveform on oscilloscope screen. Carefully sketch the waveforms (you can use oscilloscope memory function and get them in electronic form). Identify the switching threshold.

4.4. Repeat 4.3 for $V_{DD} = 10$ V, 1 V and 0.5 V. Observe change of the width of transition region ($V_{IH} - V_{IL}$), i.e. change of the inverter gain at switching threshold. Which power supply corresponds to the best inverter static voltage transfer characteristics, i.e. sharpest transition from off- to on-state? Explain why.

4.5. Select $V_{DD} = 2.5$ V again. Perform measurement of the on-state resistance r_{DSP} of PMOS. Ground inverter input. Measure output voltage. Now add a load resistor $R_L = 100$ k Ω between inverter output and ground. Measure V_{OUT} . Repeat for $R_L = 20$ k Ω , 10 k Ω and 1 k Ω . Explain change of V_{OUT} for different loads. Estimate r_{DSP} .

4.6. Perform measurement of the on-state resistances for NMOS r_{DSN} . Connect input to V_{DD} . Measure output voltage. Now add a load resistor $R_L = 100$ k Ω between inverter output and V_{DD} . Measure V_{OUT} . Repeat for $R_L = 20$ k Ω , 10 k Ω and 1 k Ω . Explain change of V_{OUT} for different loads. Estimate r_{DSN} .

4. REPORT

The report should include the lab goals, short description of the work, the experimental and simulated data presented in plots, the data analysis and comparison followed by conclusions. Please follow the steps in the experimental part and clearly present all the results of measurements. Be creative; try to find something interesting to comment on.