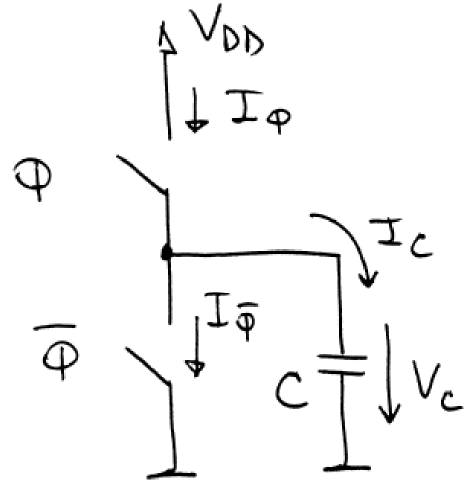
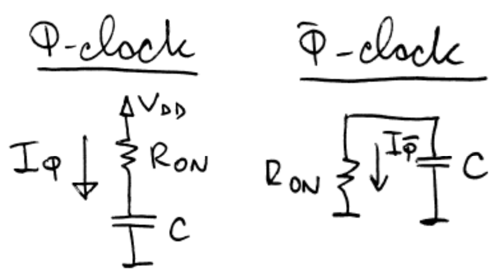
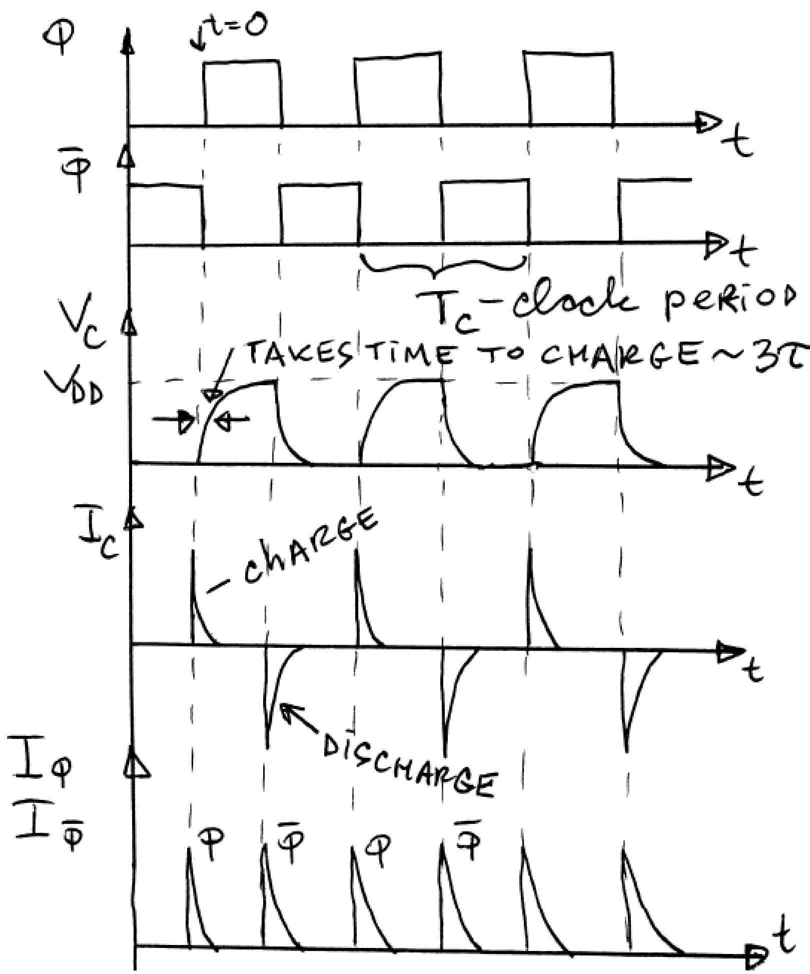
Propagation delay in digital gates

Let's first take a look at simple switched capacitor network



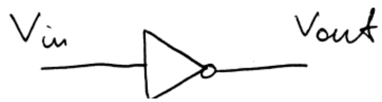


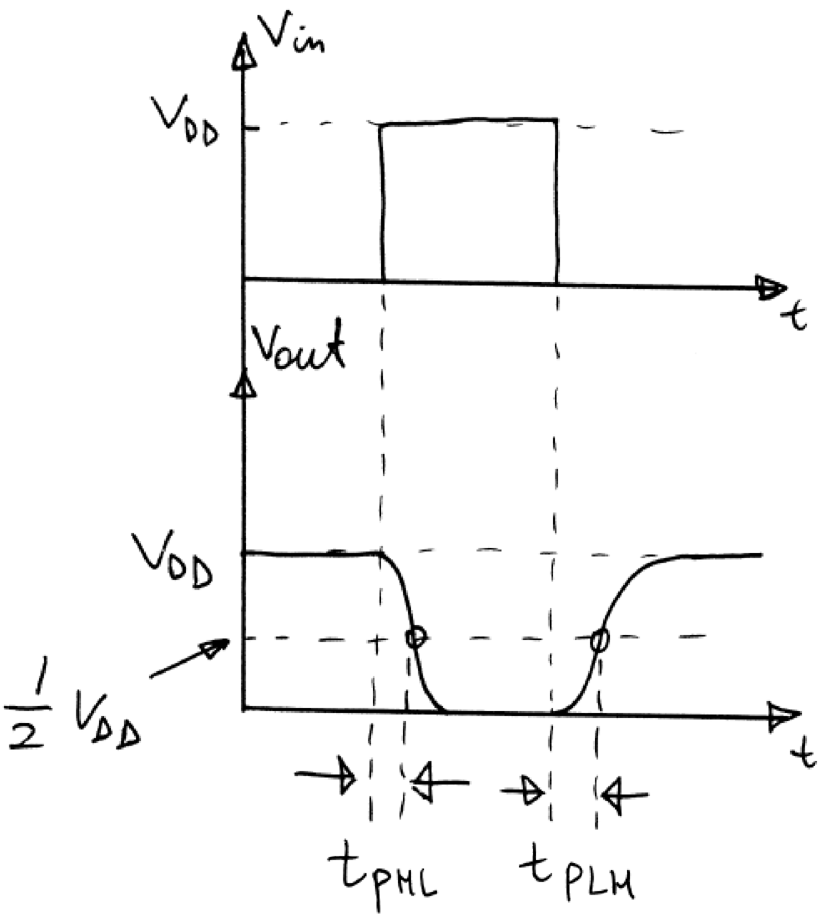


$$\tau = R_{ON} \cdot C$$

Propagation delay in inverter

Consider ideal (zero rise/fall times) input signal





Definition of inverter propagation delay

$$t_p = \frac{1}{2}\left(t_{pLH} + t_{pHL}\right)$$

Clearly, minimum clock period:

$$T_{MIN} \simeq 2\tau_p$$

And, hence, maximum clock frequency:

$$f_{MAX} \simeq \frac{1}{2t_p}$$

Power dissipation

Total power dissipated: $P_{tot} = P_{DYN} + P_{DP} + P_{stat} =$

$$= \underbrace{C_L \cdot V_{DD}^2 \cdot f}_{P_{DYN} \text{ – major part}} + V_{DD} \cdot I_{PEAK} \cdot t_s \cdot f + V_{DD} \cdot I_{OFF}$$

Power-delay product:

$$PDP = P_{tot} \cdot t_p \simeq P_{DYN} \cdot t_p = C_L V_{DD}^2 \cdot f \cdot t_p$$

For CMOS inverter operating at maximum clock frequency: $PDP \simeq \frac{1}{2} C_L V_{DD}^2$

This is energy that is being dissipated when output switches high-low or low-high:

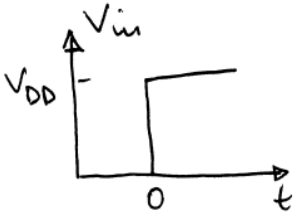
Power-delay product decreases when V_{DD} is reduced.
What about maximum operation clock?

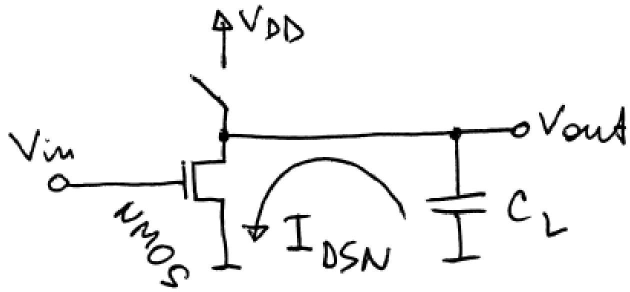
Energy-delay product: $EDP = PDP|_{\substack{max\\SPEED}} \cdot t_p = \frac{1}{2} C_L V_{DD}^2 \cdot t_p$

let's ESTIMATE t_p

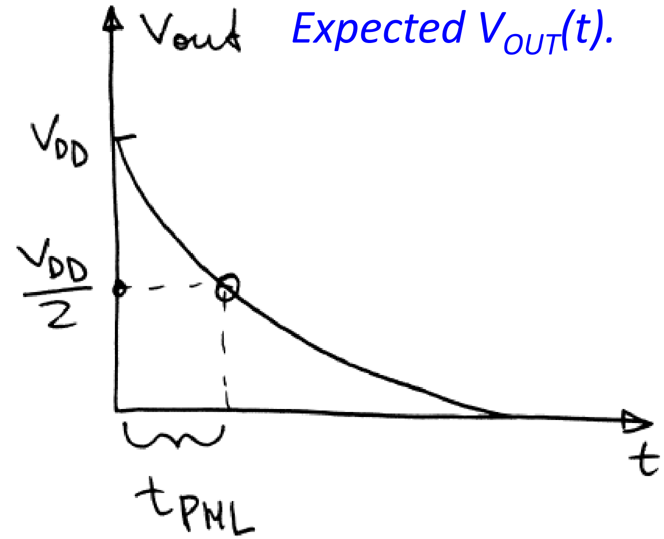
Let's first compute t_{PHL}

Still assume zero rise time of input pulse.

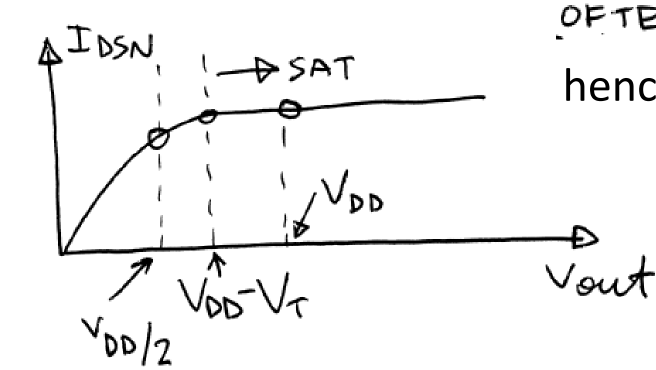




Expected $V_{OUT}(t)$.



NMOS output IV



OFTEN $V_T \approx 0.2 \cdot V_{DD}$

hence $V_{DD} > 2V_T$

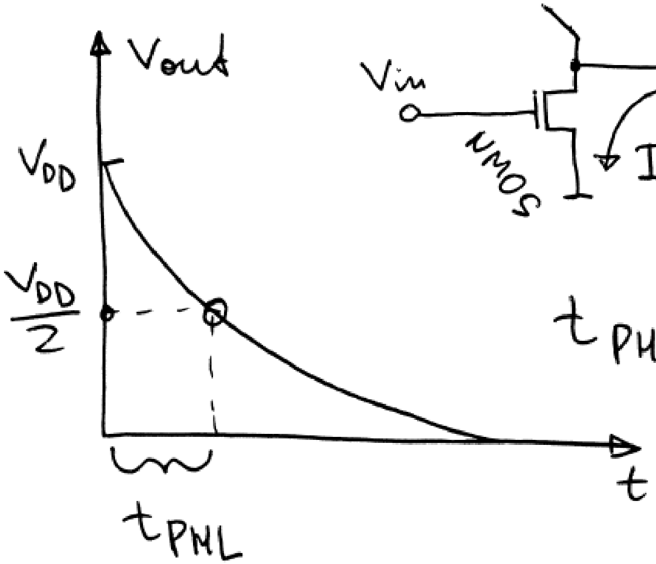
$$\frac{V_{DD}}{2} < V_{DD} - V_T$$

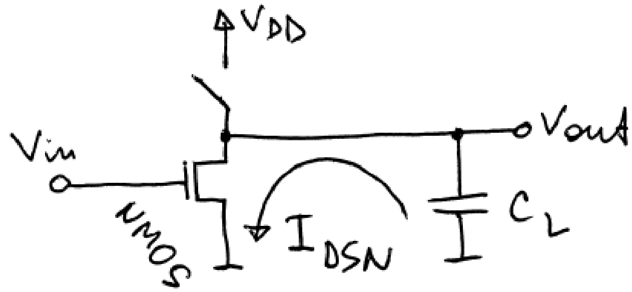
$$t = 0 \Rightarrow I_{DSN}^{SAT} \approx \frac{k_n'}{2}\left(\frac{W}{L}\right)_N (V_{DD} - V_{TN})^2$$

$$t = t_{PHL} \Rightarrow I_{DSN}^{TRIODE} = k_n'\left(\frac{W}{L}\right)_N \left[(V_{DD} - V_{TN})\frac{V_{DD}}{2} - \frac{1}{2}\frac{V_{DD}^2}{4}\right]$$

Let's first compute t_{PHL}

Approximate analysis





$$t_{PHL} \simeq \frac{\Delta Q}{\langle I_{DSN} \rangle} = \frac{C_L \Delta V_{out}}{\langle I_{DSN} \rangle} = \frac{C_L V_{DD}}{2} \frac{1}{\langle I_{DSN} \rangle}$$

$$\langle I_{DSN} \rangle \simeq \frac{1}{2}\left(I_{DSN}^{SAT} + I_{DSN}^{TRIODE} \right)$$

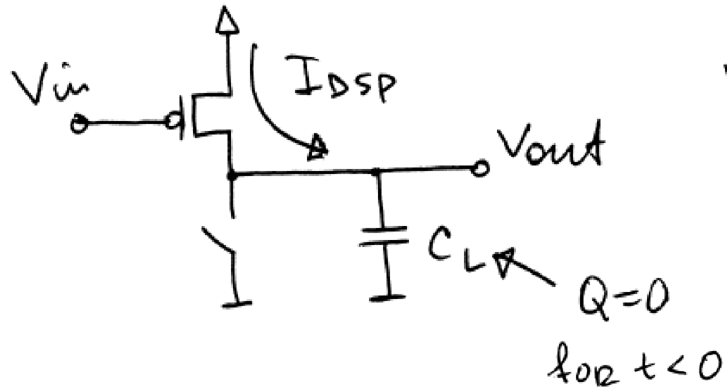
$$I_{DSN}^{SAT} \approx \frac{k_n'}{2}\left(\frac{W}{L}\right)_N (V_{DD}-V_{TN})^2$$

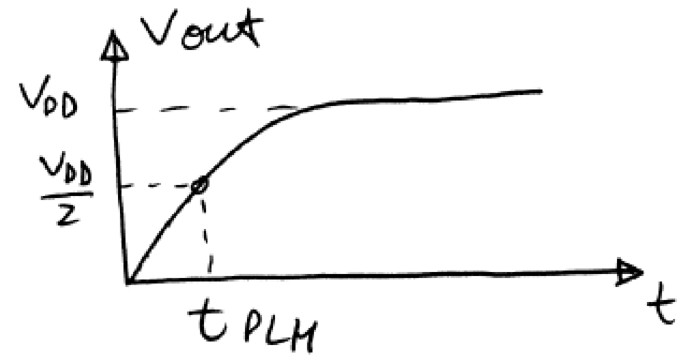
$$I_{DSN}^{TRIODE} = k_n'\left(\frac{W}{L}\right)_N \left[(V_{DD}-V_{TN})\frac{V_{DD}}{2} - \frac{1}{2}\frac{V_{DD}^2}{4} \right]$$

$$t_{PHL} \simeq \frac{\alpha_n C_L}{k_n'\left(\frac{W}{L}\right)_N V_{DD}} \quad ; \quad \alpha_n \in [1 \div 2]$$

DEPENDS ON $\frac{V_{TN}}{V_{DD}}$

Let's estimate t_{PLH}





$$t_{PLH} \simeq \frac{\alpha_p C_L}{k'_p \left(\frac{W}{L}\right)_p \cdot V_{DD}}$$

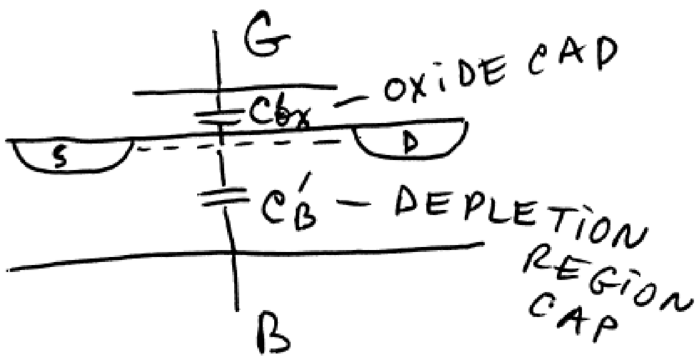
$t_{PLH} = t_{PHL}$ FOR MATCHED NMOS & PMOS $\qquad t_p = \frac{1}{2}\left(t_{PLH} + t_{PHL}\right)$

$t_p \downarrow$ when $V_{DD} \uparrow \longrightarrow$ * $P_{DYN} \simeq C_L \cdot \underline{\underline{V_{DD}^2}} \cdot f$

$\uparrow$ when $C_L \uparrow$

MOSFET capacitances revisited

Internal (fundamental)



$$Q'_I = -C'_{ox}\left(V_{GS} - V_T(V_{SB}=0)\right) - \underbrace{C'_B \cdot V_{BS}}_{\text{BODY EFFECT}}$$

Linear regime: $C_{GS} = \frac{1}{2} C'_{ox} \cdot W \cdot L = C_{GD}$

$$C_{BS} = \frac{1}{2} C'_B \cdot W \cdot L = C_{BD}$$

Saturation: $C_{GS} \approx \frac{2}{3} C'_{ox} \cdot W \cdot L$

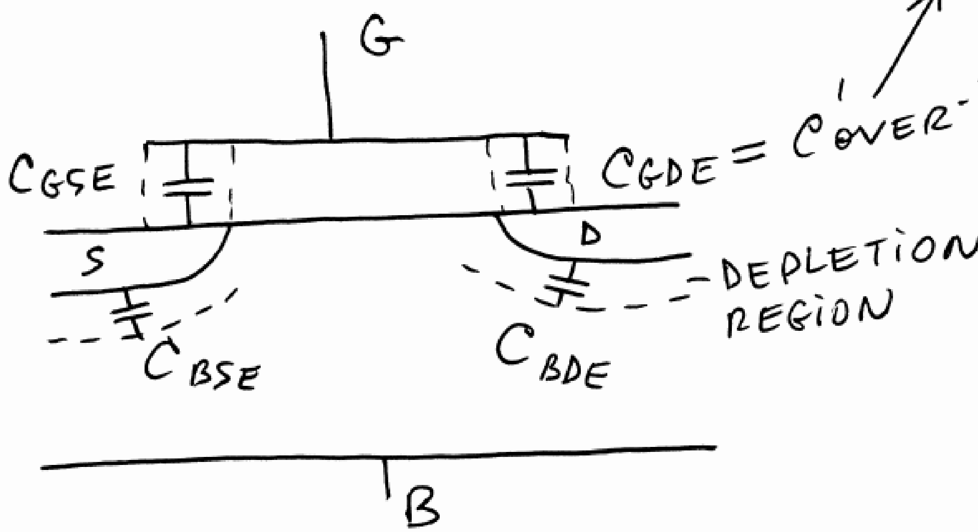
$$C_{GD} = 0$$

$$C_{BS} \simeq \frac{2}{3} C'_B \cdot W \cdot L$$

$$C_{BD} = 0$$

MOSFET capacitances revisited

External (parasitic)



$C_{GDE} = C'_{OVER} \cdot W$

$\sim 0{,}3\, fF/\mu m$ FOR $L = 0{,}25\mu$ technology

☆ C_{GDE} – Miller CAP IN CS AMP

$$C'_{\text{DEPLETION REGION}} = \frac{\varepsilon_0 \varepsilon_{si}}{W_{DEPL}(V)}$$

$$W_{DEPL} \propto \sqrt{V_{Bi} + V_{REV}}$$

$$C'_{DEPL} = K \cdot C_{jo}$$

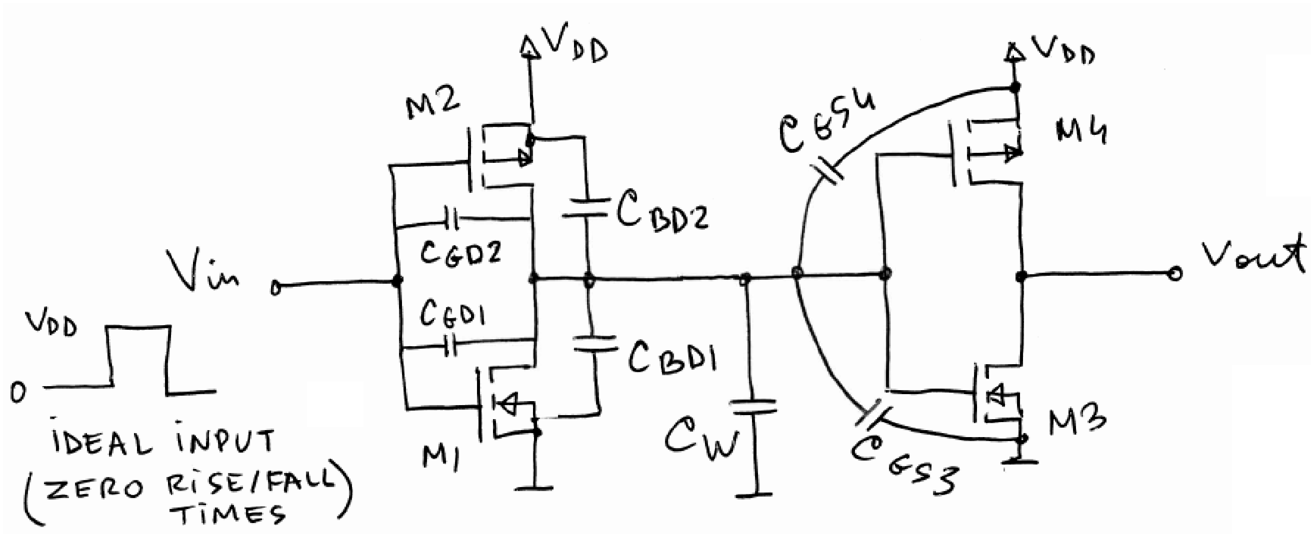
C'_{DEPL}: $\sim fF$

C_{jo}: $C_{DEPL}(V=0)$

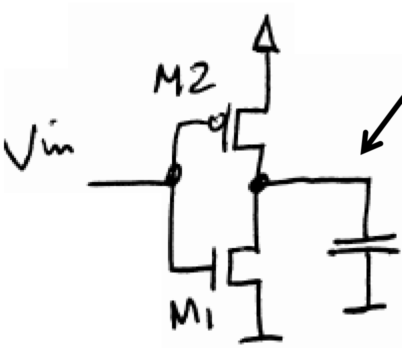
External and internal capacitances are in parallel.

Dynamic operation of CMOS inverter

Propagation delay t_P is determined when inverter drives identical inverter.



Equivalent load capacitance



2ΔV VOLTAGE CHANGE ACROSS CGD WHEN Vin CHANGES BY ΔV!

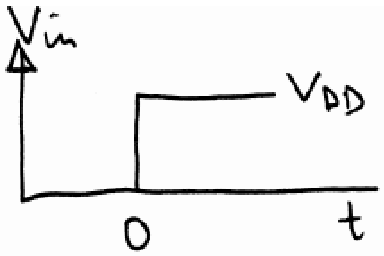
$$C_L = 2(C_{GD1}+C_{GD2}) + C_{BD1}+C_{BD2}+C_{GS3}+C_{GS4}+C_W$$

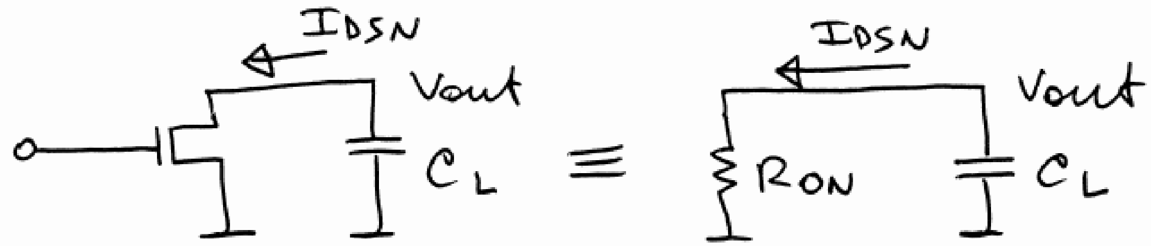
$C_L \sim 6fF$

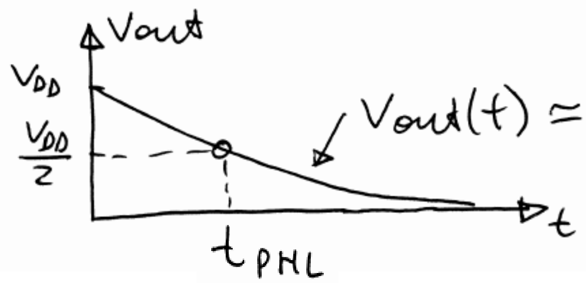
$W_p \sim 1\mu m$

MATCHED

Another popular way of estimation of propagation delay





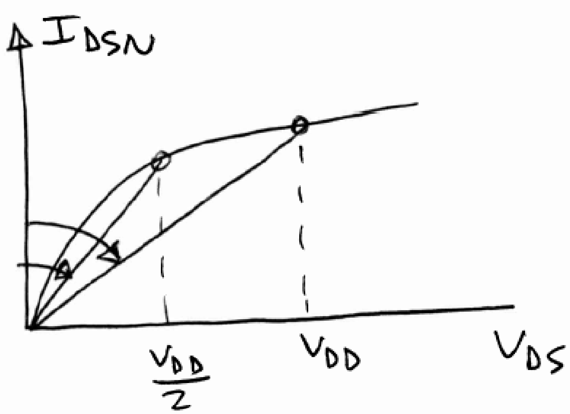


$$V_{out}(t) \simeq V_{DD} \cdot e^{-t/\tau} \Rightarrow V_{DD}\, e^{-\frac{t_{PHL}}{\tau}} = \frac{V_{DD}}{2}$$

$$t_{PHL} = \tau \cdot \ln 2 = 0{,}69 \cdot R_{ON}^{NMOS} \cdot C_L$$

Equivalently $t_{PLH} = 0{,}69 \cdot R_{ON}^{PMOS} \cdot C_L$

R_{ON} – nonlinear resistor, depends on V_{OUT}, i.e. on time



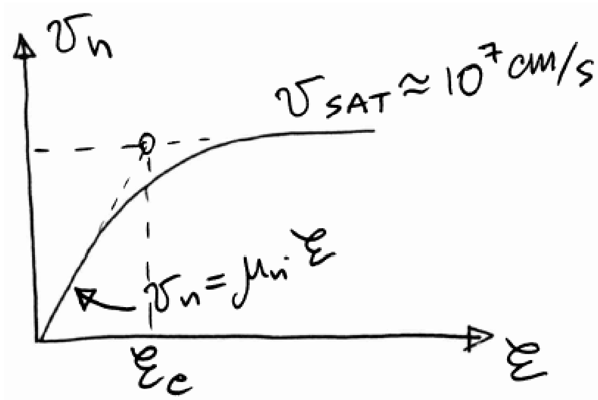
$$R_{ON} \approx \frac{1}{\Delta V} \int_{V_{DD}}^{V_{DD}-\Delta V} \frac{V_{DS}\, dV}{I_{DS}(V_{DS})} \propto \frac{V_{DD}}{I_{DS}^{SAT}}$$

$I_{DS}^{SAT} \rightarrow \sim V_{DD}^2$

$$t_p = \frac{0{,}69}{2} C_L \left(R_{ON}^{NMOS} + R_{ON}^{PMOS}\right)$$

$$t_p \sim \frac{C_L}{V_{DD}}$$

Carrier velocity saturation in MOSFET channel



$\mathcal{E}$ in channel $\approx \dfrac{V_{DD}}{L}$

when $L \downarrow \Rightarrow \mathcal{E} \uparrow$

AND CAN BECOME $> \mathcal{E}_c$

$$I_{DS}^{SAT} = \mu_n C'_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS}^{SAT} - \frac{{V_{DS}^{SAT}}^2}{2} \right]$$

$$V_{DS}^{SAT} \simeq \frac{L v_{SAT}}{\mu_n}$$

$$I_{DS}^{SAT} = v_{SAT} \cdot C'_{ox} \cdot W \left(V_{GS} - V_T - \frac{V_{DS}^{SAT}}{2} \right)$$

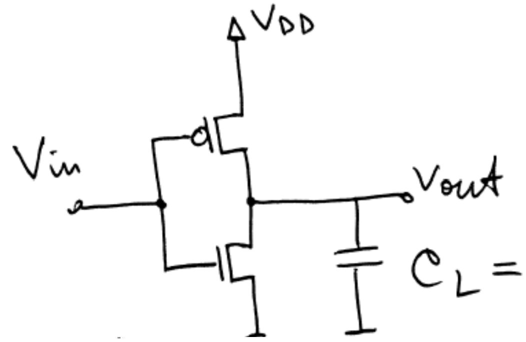
IN OUR CASE : $V_{GS} = V_{DD}$ & FOR $V_{DD} \gg V_T + V_{DS}^{SAT}/2$

$$R_{ON} \sim \frac{V_{DD}}{I_{DS}^{SAT}} \approx \frac{1}{v_{SAT} \cdot C'_{ox} \cdot W}$$

$\Rightarrow$ t_p — BECOMES "INDEPENDENT" OF V_{DD}!

(*) R_{ON} IS TOO BIG FOR $V_{DD} \leq 2V_T$

Intrinsic Delay



$$C_L = \underbrace{C_{INT}}_{=\,C_{BD}\,\&\,C_{GD}} + \underbrace{C_{EXT}}_{=\,C_{GS}\text{ OF THE NEXT INVERTER (FAN OUT) \& WIRING}}$$

$$t_p = 0{,}69 \cdot R_{ON} \cdot (C_{INT} + C_{EXT}) = \underbrace{0{,}69 \cdot R_{ON}\, C_{INT}}_{t_{p0}} \left(1 + \frac{C_{EXT}}{C_{INT}}\right)$$

MATCHED CMOS
$\Rightarrow R_{ON}^{NMOS} = R_{ON}^{PMOS}$

t_{p0} – INTRINSIC/UNLOADED DELAY

$$t_{p0} \sim R_{ON} \cdot C_{INT} \sim \frac{4\,C_{GD} + 2\,C_{BD}}{v_{SAT} \cdot C'_{ox} \cdot W}$$

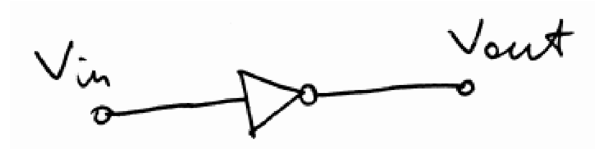
$C_{GD} = C'_{ox} \cdot W \cdot l_{OVER}$
$C_{BD} \sim W$ (pn-junction area)

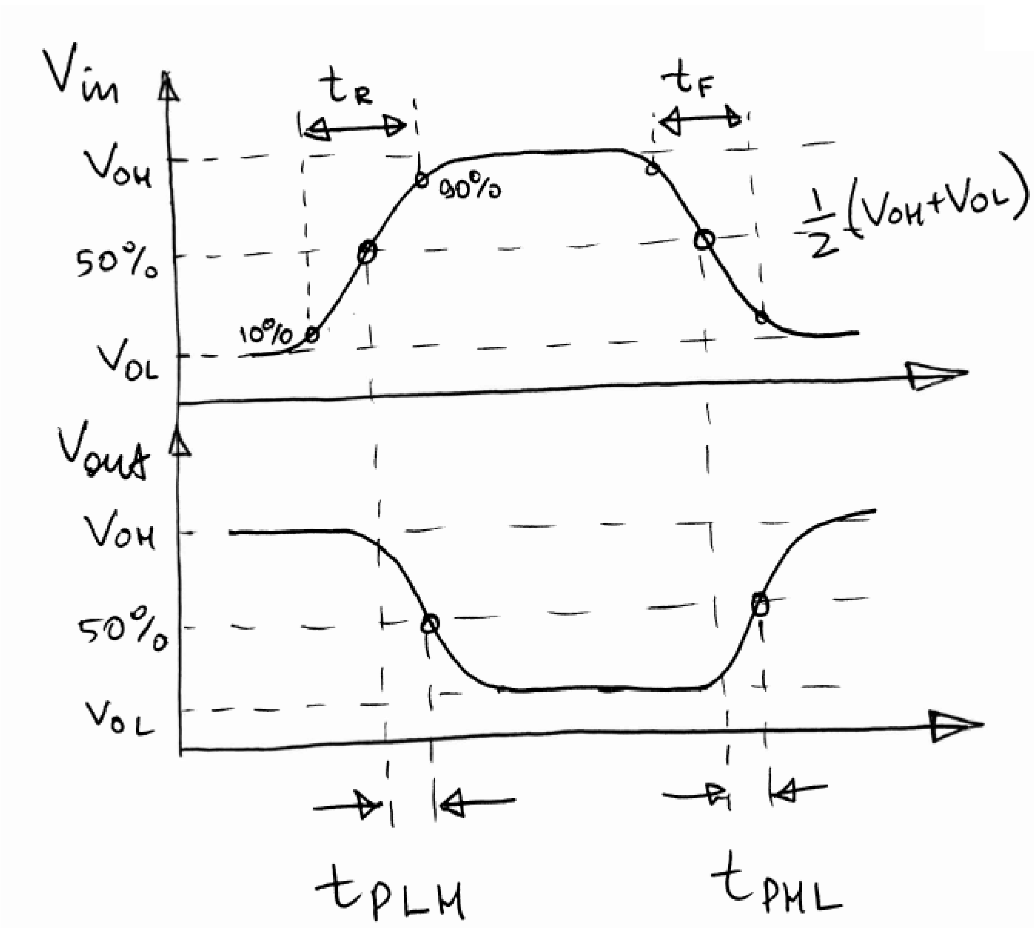
t_{p0} – DOES NOT DEPEND ON $\underline{\underline{W}}$

$$t_p = t_{p0}\left(1 + \frac{C_{EXT}}{W \cdot C_{INT}^{REF}}\right)$$

(*) FOR SMALLEST INVERTER IN TECHNOLOGY

Inverter Propagation Delay





$$t_P \equiv \frac{1}{2}\left(t_{PLH} + t_{PHL}\right)$$

$$f_{MAX} = \frac{1}{2t_P}$$

★ t_P IS LIMITED BY TIME OF CHARGE/DISCHARGE OF CAPS IN DIGITAL CIRCUIT!