Homework 1: VLSI System Design
Spring 2007; Alex Doboli
Due on Monday, Feb 12 2007

This homework has two purposes: First, to introduce you to transistor-level simulation of digital gates using IRSIM and HSPICE simulators. Second, to initiate you to the effects of transistor dimensions on digital gate speed. You will also compare the simulation accuracy of a switch level simulator, such as IRSIM, to that of a detailed circuit simulator, like HSPICE.

Switch level simulation is widely used for design and verification of the functionality and performance of digital VLSI circuits. Switch level simulation uses simplified linear models, including voltage-controlled switches, resistors and capacitors. It efficiently trades off the accuracy for faster simulation. Simulation using detailed device models offers precise performance evaluation, but it is usually not usable for large digital circuits. Simulation at higher levels of abstraction, such as gate level simulation (which you used for ESE 218), is sufficient for checking the functional correctness of a design, but is inaccurate for performance estimation. This brief discussion motivates that a digital designer should know switch level design well.

In the following homework you will assume 0.6 micron technology. The rise time is the maximum time required for the output to change from 0 logic to 1 logic. The fall time is the maximum time required for the output to change from 1 logic to 0 logic. You should submit what is in *italics*. Start early. The due that is firm.

Exercise 1) *Switch level simulation*:
a) Implement switch level models of a NOT gate and 2-input NAND gate. Using IRSIM, simulate the circuits, and make sure that they work correctly. *Submit the IRSIM source files and simulation outputs of the simulator windows showing the simulation waveforms*.
b) Attach a capacitor C to the output of each of the above circuits. Change the value of C from 80fF to 1000fF in steps of 200fF, and simulate with IRSIM. For each circuit, draw a graph with the load capacitance on the x-axis and rise-time and fall-time on the y-axis. *Submit the graphs*. *In your opinion, what is the mathematical relationship between fall and rise times and the value of C?*
c) Implement a 3-input NOR gate. Attach a 100fF capacitor at the output of the gate. Keep the lengths of the transistor constant at 0.6microns, and modify the widths such that both the rise-time and fall-time become 0.4ns. Increase C to 1000fF in steps of 300fF. In each case, modify the transistor widths such that the fall-time and rise-time remain 0.4ns when measured with IRSIM. Draw the graph with the capacitance in the x-axis, and W_n/L_n and W_p/L_p on the y-axis. *Submit the graph. How is the W/L ratio changing with C?*
d) Attach a 300fF capacitor to the output of the NOT and NAND gates. Size the transistor widths such that both the rise-time and fall-time are 0.3ns when measured with IRSIM. *Draw the circuits, and indicate the transistor width value for each transistor. Why is the PMOS transistor larger than the NMOS transistor?*
e) For 1.0 and 2.0 micron technologies, simulate the NOT and NAND gates having the 500fF capacitor at the output. The transistor dimensions are those found at Exercise 1.d. *Indicate the fall-time and rise-time for the two technologies. Explain how the speed of a circuit is changed depending on the technology.*

Exercise 2: *Detailed Level Simulation:*
HSPICE is a simulator that uses detailed electrical models for the devices than IRSIM.

a) Simulate the NOT and NAND circuits sized at Exercise 1.d using HSPICE. *Compare the rise-time and fall-time obtained with HSPICE to those obtained with IRSIM. What is the error? Is this error tolerable in practice?*
b) Resize the transistor widths such that the rise-time and fall-time are 0.3ns. *Submit the HSPICE waveforms and the final transistor sizes.*

Summarize what you have learned from these two exercises. Your summary should be organized as a list of items and rules of thumb, which you could use in the future.