GETTING STARTED WITH HSPICE – A TUTORIAL

Charles R. Kime Dept. of Electrical and Computer Engineering University of Wisconsin – Madison

INTRODUCTION

A SPICE (HSPICE) simulation has three primary steps:

- 1) Generating the circuit netlist file,
- 2) Running the simulation, and
- 3) Displaying, analyzing, and printing the simulation results.

In this tutorial, we will carry out these three steps for an implementation of an Exclusive OR gate made up of four NAND gates. Since this is a digital circuit, digital electronic circuit simulation techniques are used rather then analog techniques used in other electronics courses. Some differences are:

1) Input waveforms: DC, PWL (Piece-Wise Linear) PULSE versus

AC, DC, SIN, EXP.

2) Analysis: DC and TRAN vs. OP, AC, FOUR, NOISE,

SENS, etc.

3) Circuit Elements: V, F(I-controlled I source), C, R,

M(MOSFET), Q(BJT), T(Lossless line), U(Uniform RC line).

The EXOR gate will be hierarchical – made of 4 NAND gates – as shown in Figure 1a). The logic and circuit design has been completed. In addition, we have enough of a layout to estimate the areas and perimeter of the sources and drains and the capacitive loading on the circuit within an IC.

DEVICE MODEL FILES

You are to establish your own directory and collection of device models for MOSFETS and other devices.

- 1. Make a directory for SPICE models. Suggested name: spice_models.
- 2. Open Netscape and go to the ECE 555 Contents and Links page.
- 3. Open HSPICE Level 13 for 0.6 micron CMOS Process.
- 4. Save as scn06hp.L13 in your SPICE models directory.

FILE GENERATION

The netlist file is made up of statements. A SPICE file is case-insensitive except for file names exported to UNIX as in a .include or .lib statement. * in the left column designates a comment.

Netlist Structure:

Title (Required) Circuit Subcircuit(s) Device Models Analysis Output . end (Required)

File Entry for the Example
1. Make a directory for the files for this tutorial.
2. Edit the netlist file design.sp.
3. Enter title.
4. Enter the Exclusive OR circuit made up of NAND subcircuits. Assume that the statement for the NAND subcircuit is:

Xi top_in bot_in out NAND

The component labels and input and output nodes to appear in the above statement for each gate can be obtained from Figure 1a). Example statement:

X1 101 102 103 NAND

Note that GND is always node 0 and that we will reserve node 1 for VDD.

5. Enter the subcircuit for the NAND gate.

a. Declare the subcircuit by entering:

.SUBCKT NAND top_in bot_in out

FILE GENERATION

FIGURE 1-1

Tutorial Circuit

a) Logic Design – EXOR:



b) Circuit Design – NAND 2:



c) Simulation Environment – EXOR:



b. Enter each of the four MOSFETs using the node numbers given in Figure 1b). The format for a MOSFET is:

(1) Name beginning with M

(2) Node numbers: Drain Gate Source Base

(3) MOSFET model name

(4) Length L= and Width W=

OPTIONAL:

(4) Areas of Drain and Source: AD AS

(5) Perimeters of D and S: PD PS

(6) No. of squares of D and S Resistance NRD NDS

(7) OFF - initial condition spec for DC or

IC = (VDS, VGS, VBS) for .tran with UIC (use initial conditions) in the .tran command. This uses specified initial conditions instead of solving for initial quiescent operating point. Also, one can use separate commands called .NODESET for DC and tran to initialize the circuit - e.g., circuit with flip-flops.

(8) TEMP, which is the transistor temperature if other than 25 degrees C.

The entry for the p-channel MOSFET M1 is:

M1 out top_in 1 1 tp L=0.6u W=1.2u + AD=2.88p AS=2.88p PD=7.2u PS=7.2u

M3 and M4 use the n-channel MOSFET model name tr.

c. Add .ends NAND to end the subcircuit.

6. Enter the remainder of the circuit consisting of the simulation environment in Figure 1c). Enter VDD connected from node 1 to node 0 with a value of 3.3 volts and the load capacitance C1 with a value of 0.01pf. Also, enter thestatement:

.GLOBAL 1

This statement causes all nodes numbered 1, whether in the main circuit or a subcircuit, to be connected together. In this case, a common node for VDD is formed. Otherwise, it would be necessary to make node 1 a parameter in the subcircuit header and include it in each call to the subcircuit.

For the remainder of the netlist file, we need to consider what we wish to evaluate:

1) correct function? Yes - need to apply all combinations of H and L values.

(2) noise margins? Yes - need to find VTC using DC sweep.

(3) propagation delays and rise and fall times? Yes - need to apply PULSE or PWL waveform.

(4) Power dissipation? Yes - need to apply PULSE or PWL waveform carefully and do a power measurement.

The format for a PULSE is:

vname n+ n- PULSE(V1 V2 TD TR TF PW PER)

How wide should each interval be? Enough to allow events to complete before next input event occurs. Often useful to draw to scale first.

Enter pulses VA and VB:

VA 101 0 PULSE(0 3.3 0n 0.2n 0.2n 4.8n 10n)

VB 102 0 PULSE(0 3.3 2.5n 0.2n 0.2n 4.8n 10n)

7. Enter statement to include the transistor models:

.LIB '/your_path_name/spice_models/scn06hp.L13' NOM

If you don't know your path name, enter pwd to display it.

In this case, we have used a library statement that permits different model sets within the same file. In this case, the NOM (standing for nominal) set of models is selected.

8. Enter analysis and output commands.

For the VTC, the form of the DC sweep is:

.DC srcnam vstart vstop vincr (src2 start2 stop2 incr2)

Enter:

.DC VA 0 3.3 0.01 VB 0 0 0.01

to give the transfer characteristic with only VA changing. To indicate the output needed, **enter:**

.PROBE V(106)

For the function and delay, the form of the transient command is:

.TRAN tstep tstop (tstart tmax) (tmax is no of steps within tstep)

Enter:

.TRAN 0.01N 20N

tstep should be about 1/10 of what you want as the least significant position's value in the result. Here we want result to 0.1ns. Note that in this case, the analysis will produce 2000 points. To limit outputs to those needed, **enter:**

.PROBE V(101) V(102) V(106)

To find the average power consumption, enter:

.MEASURE avg_pow AVG power FROM=10n TO=20n

power is a keyword that represent the instantaneous power dissipation for the circuit.

In order to cause .PROBE to have an effect, to prepare outputs for MetaWaves, and to produce .MEASUREMENT outputs, enter the following statement:

.OPTIONS PROBE POST MEASOUT

9. Finally, enter . END to complete the netlist file.

If you do not feel that you have a well-formed HSPICE file, copy the file from:

```
~kime/public_html/555/tutorials/sp_tu_ex.sp
```

for use in the rest of the tutorial.

RUNNING THE SIMULATION

Have at least two Xterm windows open and the directory set to that containing your design.sp file. In one of the Xterm windows, **enter:**

rm design.lis

Later, entering:

!r

will be used to delete the design.lis file before each run of HSPICE.

In the other window, launch MetaWaves by entering;

mwaves

In MetaWaves, click **Design:Open**. Select design.sp and click on **OK**. A message will appear saying "No data in design" Click on **OK**. In order to generate data, run HSPICE by clicking **Tools:Run HSPICE**, selecting design.sp and clicking **Run**.

When **Done** appears, continue at *DISPLAYING*, *ANALYZING* AND *PRINTING RESULTS*. If **Error** appears, then click on **Listing**. In the design.lis file, search for the word "error." You will find a terse explanation of the problem or problems. In the Run Manager window (which you may have to relaunch by clicking **Tools:Run HSPICE**), click on **Source** and edit your design.sp file to correct the error(s).

Then go to the other Xterm and enter !r to delete the design.lis file. (If you do not do this, HSPICE will not produce new output files.)

In the Run Manager, click on Run. Repeat the above until you have no errors.

DISPLAYING, ANALYZING, AND PRINTING RESULTS

First, to get the current version of the waveforms, click on **Panels:Update**. The go to the **Results Browser** and select the DC analysis. Under **Types**, select **Voltages** and in under **Curves** select v(106) and use the middle mouse button to drag it to the **Results Panel**. The waveform appearing is the VTC (Voltage Transfer Characteristic) for the EXOR.

We now want to make a measurement used to find noise margins. Specifically, we want to find V_{IL} and V_{IH} , the input voltages at which the VTC has slope (derivative) +1. To find these points, we will first find the curve for the derivative of the VTC. Then we will

find the two points at which the value is +1 and measure the input voltage at those points.

Click on **Tools:Expressions**. In the **Expression Builder** window, select derivative(_) in the **Functions** area and, using the middle mouse button, drag it to the **Expression:** area at the top of the window. Next select v(106) in the **Results Browser** window and drag it to the point between the parentheses in the **Expression:** area. Enter the variable name slope in the **Result:** area and click on **Apply**. slope will now appear in the **fd**area. Select it, and using the middle mouse button, drag it to the panel.

Note the scale on the right. Since it ranges from 0 to around 120, it will be very difficult to find the +1 value. To zoom in on the +1 level on the derivative curve, click on the \mathbf{Y} + **zoom in** shortcut and draw a short line with the cursor between roughly 4 and 0. Repeat \mathbf{Y} +, drawing a line between 2 and 0.

Next, click on **Measure:Measure Label Options**, select **Current X** and enter VIL in the text area next to it and click **OK**. Then click on the **Point** shortcut and place the cursor on the left +1 slope point and click. The value of V_{IL} for the noise margin calculation will appear. Repeat, entering VIH and using the right +1 slope point. By careful use of such features, you can very neatly annotate your plots and printouts.

To examine printing options, click on **Tools:Print**. Note the various options. Click on **File** to see the options for printing to a file. Warning: Do not select **Landscape** when printing to a file; you will be unhappy with the results.

To return to a full view of the VTC, click on Window:Full.

Next we want to look at the transient analysis results. Click on the V(106) entry in **Wave** List and then on **Panels:Delete Curves** to remove the VTC from the **Results Panel**.

In the **Results Browser**, select the transient analysis. Select **Voltages** in **Types**, and select and drag to the **Results Panel** the voltages V(101), V(102), and V(106). In the **Wave List**, click on V(106) to highlight it. Drag across all three voltages to highlight all. Then click on V(106) again. To highlight only V(101) in addition to V(106), hold down Control and then click on V(101).

With V(101) and V(106) highlighted, we want to evaluate some delays. Click on **Measure: Measure Label Options** and select **Delta X**, deselecting all others. Click on **OK**. To set the voltage level at which to measure the delay, click on **Measure: Measure Preferences**. Select **Lock Horizontal at Y** and enter 1.65 which is 50% of 3.3. Click on <u>OK</u>. Click on the **PointtoPoint** shortcut, place the marker on V(101) and drag to V(106). The value displayed is the rising or falling propagate delay from input A to the Output with B at its value at the time of the measurement. Next, try to measure the risetime for V(106).

Suppose that you want to display V(101), V(102), and V(106) so that they are more readable for functional verification. We will use **Expressions** to do this. To separate the waveforms, we will add 12 to V(101), 8 to V(102), and 4 to V(106). To add 12 to V(101), click on the **Expressions** shortcut. Drag V(101) from the **Curves** area to the **Expression** area, type + followed by 12. Enter A in the **Result** area and click on **Apply**. Perform similar operations for V(102) and V(106), naming the results B and OUT, respectively. Then drag A, B, and OUT to the **Result Panel** for display.

For the final measurement, use **Add Panel** on the **Panel List** to add a second panel. In the **Results Browser**, click on **Measures** in **Types**. Drag avg_pow to the new panel. The

average power has no curve, but the value is that listed closest to the center of the vertical axis. Do not attempt to place a second scalar measure on a panel; to see what happens, drag temper to the panel. Is 25 degrees at the center of the panel?

To exit MetaWaves, **enter Design:Exit**. Save the configuration if you want to archive information generated during the session such as expressions, macros and waveforms derived from the basic waveform data. These can be used in a later session for the same design by opening the same configuration.

For more information on HSPICE, enter the following:

cd /afs/engr.wisc.edu/apps/hspice/97/docs/hspice/Publish
viewer

or

cd /afs/engr.wisc.edu/apps/hspice/97/docs/hspice/Postscript

ghostview

For more information on MetaWaves(AvanWaves), see the on-line help or use ghost-view on the following:

/afs/engr.wisc.edu/apps/hspice/97/docs/rel_notes/AvanWavesUG.97.2.ps

APPENDIX - THE EXAMPLE SPICE FILE

```
2-input All-nand-gate Exclusive OR
*In ~kime/public_html/555/tutorials/sp_tu_ex.sp
*1/23/97
*Define EXOR Circuit
*Four NAND Implementation
*Node 101 Is Input A, node 102 Is Input B, node
*106 Is Output
X1 101 102 103 NAND
X2 101 103 104 NAND
X3 103 102 105 NAND
X4 104 105 106 NAND
*Define subcircuit NAND
.SUBCKT NAND top_in bot_in out
*Node 1 is VDD; node 0 is GND
M1 out top_in 1 1 tp L=0.6U W=1.2U
+AD=2.88p AS=2.88p PD=7.2U PS=7.2U
M2 out bot_in 1 1 tp L=0.6u W=1.2U
+AD=2.88p AS=2.88p PD=7.2U PS=7.2U
M3 out top_in 2 0 tn L=0.6U W=1.2U
+AD=2.88p AS=2.88p PD=7.2U PS=7.2U
M4 2 bot_in 0 0 tn L=0.6U W=1.2U
+AD=2.88p AS=2.88p PD=7.2U PS=7.2U
.ENDS NAND
*Power and load and input signals
VCC 1 0 DC 3.3
C0 106 0 0.01p
.GLOBAL 1
VA 101 0 PULSE(0 3.3 On 0.2n 0.2n 4.8n 10n)
VB 102 0 PULSE(0 3.3 2.5n 0.2n 0.2n 4.8n 10n)
*Include MOSFET Models
.LIB '/pong/usr5/k/kime/spices/scn06hp.L13' NOM
**Specify analysis and display
.DC VA 0 3.3 .01 VB 0 0 0.1
.PROBE V(106)
*Delays and Power
.TRAN .01N 20N
.PROBE V(101) V(102) V(106)
.MEASURE avg_pow AVG power FROM=10n TO=20n
.OPTIONS PROBE POST MEASOUT
.END
```

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