High transconductance and large peak-to-valley ratio of negative differential conductance in three-terminal InGaAs/InAlAs real-space transfer devices

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Three-terminal real-space transfer devices with improved room-temperature characteristics have been implemented in InGaAs/InAlAs/InGaAs heterostructures lattice matched to InP. The devices exhibit extremely sharp charge injection, characterized by a transconductance exceeding 23 S/mm and a negative differential conductance with a peak-to-peak ratio of over 7000. Our experiments suggest that both of these characteristics are limited only by the dielectric strength of the InAlAs barrier layer.

The charge-injection transistor (CHINT) and the negative resistance field-effect transistor (NERFET) are two modes of operation of a three-terminal heterostructure device (Fig. 1) based on the real-space transfer (RST) of hot electrons between two conducting layers. One of these layers ("emitter") has source and drain contacts and plays the role of a hot-electron cathode. The other layer ("collector") is separated by a potential barrier and draws little current, unless electrons are heated by the source-drain field. When that happens, however, most of electrons do not reach the drain but are injected into the collector layer. A strong negative differential resistance (NDR) develops in the drain current (I_D) characteristic (the NERFET action). Control of the injection (the CHINT action) allows the implementation of novel circuit elements. In particular, we have proposed and experimentally demonstrated a single device structure that performs such logic operations as NOR and AND with a fast switching between these functions.[1]

Recently, we reported[2] the first successful implementation of CHINT/NERFET devices in the InGaAs/InAlAs system lattice matched to InP. Advantages of this system for RST transistors stem from the low effective electron mass $m = 0.042\ m_0$ in the Γ valley of InGaAs, the high conduction-band discontinuity ($\Delta E_C \approx 0.5$ eV), and the still higher satellite-valley separation ($\Delta E_{\Gamma L} \approx 0.55$ eV).[3] Although these advantages were apparent a long time ago, they had not been exploited until recently because of the difficulties in implementing nonshorting ohmic contacts. This essential problem was solved with the help of nonalloyed epitaxial contacts. The present letter reports a further modified device structure with enhanced CHINT/NERFET characteristics.

The heterostructure has been grown by molecular beam epitaxy (MBE) at 550 °C on a semi-insulating iron-doped InP(100) substrate. It consists of the following layer sequence (Fig. 1): a 5000-Å-thick n^+-$In_{0.53}Ga_{0.47}As$ collector layer followed by a 500-Å-thick lightly doped n^--$In_{0.53}Ga_{0.43}As$ setback layer, a 2000-Å-thick undoped $In_{0.52}Al_{0.48}As$ barrier layer, and a lightly doped 500-Å-thick $In_{0.53}Ga_{0.47}As$ emitter layer, followed by a 25-Å-thick n^+-$In_{0.52}Al_{0.48}As$ etch-stop layer, and an ultraheavily doped (Sn) 200-Å-thick $In_{0.53}Ga_{0.47}As$ cap layer.

Figure 1 shows a cross section of the device obtained after several wet chemical etching and ion milling steps. All patterns were defined by the standard optical contact lithography, including the critical definition of a trench separating the source and drain areas. This trench, 200 Å deep, defines the emitter channel. It is obtained by a highly selective wet chemical etching of $In_{0.53}Ga_{0.47}As$, which stops reliably at a 25-Å-thick $In_{0.52}Al_{0.48}As$ layer introduced especially for that purpose. For different devices, the trench length L_{ch} varied from 0.6 to 5 μm, and the trench width W varied from 25 to 75 μm. After etching, the exposed portion of the channel is entirely depleted by the surface potential, but with a positive voltage applied to the collector, a two-dimensional electron gas is induced in the channel, as illustrated in Fig. 1. Contacts to the channel were ohmic down to liquid-helium temperatures.

The 25-Å-thick InAlAs etch-stop layer is one of the modifications of our present structure compared to earlier work.[2] We found no degradation of the contacts from the introduction of this layer. Another new element in the structure is the lightly doped setback layer between the barrier and the collector. Its purpose is to reduce the possibility of unintentional doping of the barrier during MBE growth by an out-diffusion of donors from the collector.

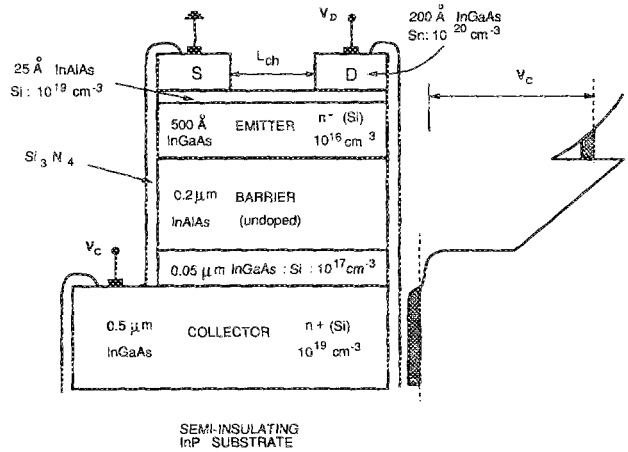

FIG. 1. Cross section of the device structure and the energy-band diagram under an applied collector bias. The trench in the heavily Sn-doped cap layer defines the emitter channel.

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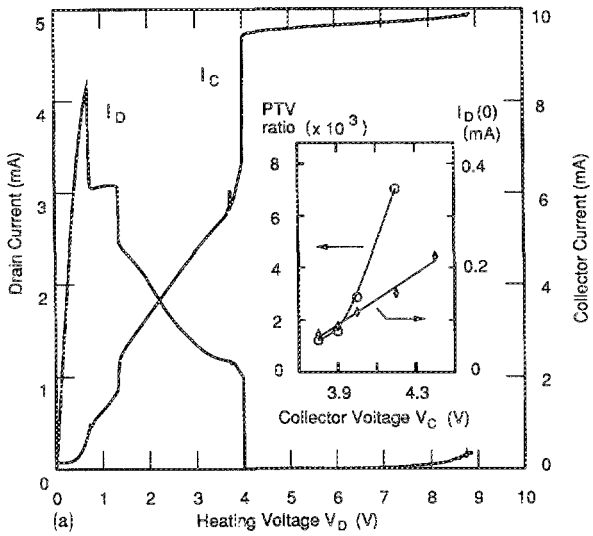

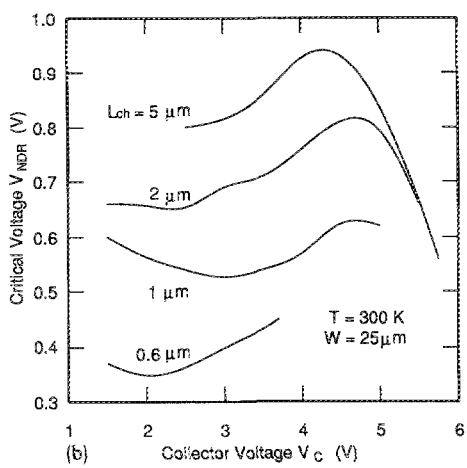

FIG. 2. Basic device characteristics at 300 K: (a) Drain current (I_D) and collector current (I_C) vs the heating drain voltage V_D at a fixed collector bias $V_C = 3.9$ V for a device with $L_{ch} = 1$ μm. (Inset) Collector-bias dependence of the peak-to-valley ratio and the leakage current, defined as the magnitude of I_D at $V_D = 0$. (b) Collector-bias dependence of the critical voltage V_{NDR} (the value of V_D at the peak of I_D) for various emitter channel lengths L_{ch}.

Compared to our earlier report, the dielectric strength of the barrier is substantially enhanced (see below) and we attribute this improvement to the presence of the setback layer.

Figure 2 describes the current-voltage characteristics of 25-μm-wide CHINT/NERFET devices at $T = 300$ K. The striking feature of the present devices is a NDR in the drain characteristic with a peak-to-valley (PTV) ratio typically exceeding 1000 at room temperature. In contrast to most of the previous studies of the device, this strong NDR is obtained in the presence of a low leakage current due to "cold electrons". As the plot in Fig. 2(a) illustrates, the NERFET switches almost the entire source current from the drain branch of the biasing circuit to the collector branch. The resulting collector current, I_C, is more than two times larger than the peak value of I_D.

As the inset to Fig. 2(a) shows, both the leakage current and the PTV ratio are increasing functions of the collector voltage. At $V_C = 4.4$ V, the observed PTV exceeds 7000. Our measure of the leakage is the value of I_D at $V_D = 0$; in a perfectly symmetric device it equals half the value of I_C at the same bias. Within the limit of V_C imposed by a dielectric breakdown of the $In_{0.52}Al_{0.48}As$ layer, we observed no tendency toward saturation in either PTV or $I_D(0)$. It is likely that the present order-of-magnitude improvement in PTV over our earlier devices[2] can be attributed to the introduction of the 500-Å-thick lightly doped $In_{0.53}Ga_{0.47}As$ setback layer that suppressed the outdiffusion of Si from the collector region to the barrier. The dielectric strength of the barrier and its abruptness at the collector side is thereby increased, as evidenced not only by the smaller leakage at low V_D but also by a broader valley in I_D at high drain biases. As seen in Fig. 2(a), this valley persists up to $V_D - V_C \approx 5$ V, until it is overwhelmed by an injection of "cold electrons" from the collector.

The CHINT common-source characteristics, $I_C(V_C)$ at fixed values of V_D, have been discussed in Ref. 1. The variation of V_C affects not only the PTV ratio but also the critical voltage, V_{NDR}, for the onset of NDR. The basic trends in the dependence of V_{NDR} on V_C at different emitter channel lengths L_{ch} are shown in Fig. 2(b). The L_{ch} dependence at low V_C is qualitatively clear: the electron temperature in the channel is controlled by the drain field which at a fixed V_D increases with decreasing L_{ch}. In devices with $L_{ch} = 0.6$ μm, the onset of the NDR is observed at drain voltages as low as 0.34 V. Such a low V_{NDR} in NERFET devices has not been reported before. Note that this V_{NDR} includes the voltage drop in the contacts but still is appreciably lower than the barrier height $\Delta E_C/e \approx 0.5$ V. This provides strong evidence that the RST proceeds from the tails of a "thermalized" hot-electron distribution function rather than by a single-event scattering of ballistically accelerated electrons.

As seen from Fig. 2(b), increasing the collector bias first results in a slight downward shift of V_{NDR}, but this trend reverses at $V_C \gtrsim 2.5$–3.0 V. The initial decrease can probably be explained by a rise in the channel mobility as the carrier concentration is enhanced by V_C. The subsequent upward shift in V_{NDR} can be understood in analogy to the increase of the "pinch-off" voltage at higher gate biases in a typical FET. Indeed, at $V_C \gtrsim 2$ V the onset of RST occurs in the same range where the I_D–V_D characteristics typically begin to saturate—suggesting that the process initiates in a pinch-off region near the drain. Finally, we see from Fig. 2(b) that at higher collector voltages the V_{NDR} shifts back to lower values. Noting that this shift occurs in the region $V_C \gtrsim 4.5$ V where the leakage of cold electrons from the emitter channel is substantial, we explain it by the increased importance of the tunneling process in the RST.[4] At high V_C, the charge injection occurs via "thermally" assisted tunneling. This is equivalent to an effective lowering of the barrier height; a given RST current is therefore realized at a lower electron temperature, and hence at a lower V_D.

An important figure of merit for any transistor is its transconductance, g_m. For the CHINT, it is defined as the slope of the I_C vs V_D characteristic at a constant V_C per unit width W of the emitter channel: $g_m \equiv W^{-1} \partial I_C / \partial V_D$.

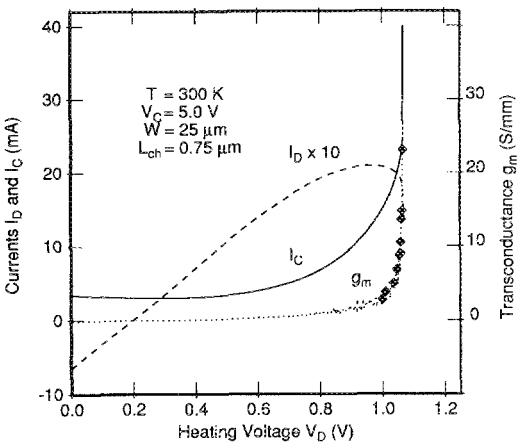

FIG. 3. Drain current I_D, collector current I_C, and the transconductance g_m, as functions of the drain voltage at a high collector bias $V_C = 5.0$ V. Large enhancement in the transconductance, g_m, is observed at $V_D > V_{NDR}$ in the stable NDR region. Diamonds represent the actual discrete data points for g_m in that region obtained by a numerical differentiation of the I_C curve.

The highest previously reported CHINT transconductance, $g_m \approx 1\,000$ mS/mm, was obtained by Kastalsky *et al.*[5] in GaAs/AlGaAs CHINT/NERFET devices. The transconductance characteristics of our present devices are shown in Fig. 3, which plot the V_D dependence of I_D, I_C and g_m at a fixed collector bias $V_C = 5.0$ V. We see that in a narrow range of V_D above 1 V the injection current rises by an order of magnitude, leading to an extremely high $g_m = 23.1$ S/mm. When the injection current exceeded certain limit (≈ 50 mA for 25 μm devices), the InAlAs barriers usually suffered a dielectric breakdown. Therefore, we had to limit the I_C: the data presented in Fig. 3 were collected with a compliance set at 40 mA. The large boost in the injection current is observed within a range $V_D = 1.02$–1.03 V right after V_{NDR}, but before the onset of circuit oscillations caused by the NDR. The existence of a stable NDR region has been observed only at large values of V_C. We believe that the ultrahigh transconductance is related to the formation of a high-field RST domain in the channel. It appears that at high values of V_C the domain formation in our devices occurs continuously as a function of V_D. In a narrow range of V_D, corresponding to the stable NDR, the source-to-drain electric field (initially, relatively uniform over the channel because of the high-carrier concentration) concentrates in a "hot spot" (the domain) depleted to carriers.[2] A small variation of V_D reduces the domain size, thus producing a large change in the electric field, hence a large variation in the electron temperature and the injection current that gives rise to a high g_m.

Although the idea of a continuous domain shrinkage is highly speculative and certainly warrants further study, we stress that some sort of a cooperative process is likely to be required in order to explain the observed ultrahigh values of g_m. Our understanding in terms of a global charge redistribution in the device (the "avalanche" RST process)[2] is reasonable, especially in light of the results of Monte Carlo studies of CHINT/NERFET.[6] What we find most intriguing, however, is the continuous nature of the domain formation, albeit in a narrow range of V_D. The measured characteristics in this range are highly reproducible with no sign of hysteresis. Microwave studies of CHINT are underway. Our recent experiments[7] demonstrate excellent high-speed performance of the device: a current gain with $f_T \approx 40$ GHz and the unity maximum available gain at frequencies exceeding 25 GHz. The measured gain cutoff frequencies exceeded ~ 20 GHz in a range of V_D at least 0.5 V wide and a still wider range of V_C.

In conclusion, we have reported dc measurements in InGaAs/InAlAs CHINT/NERFET devices of an improved design. In these devices, the peak-to-valley ratio of the negative differential resistance in the drain circuit routinely exceeds 1000, with a maximum observed value of 7000. The measured peak transconductance typically exceeds 10 S/mm, the highest observed value being $g_m = 23.1$ S/mm. We observed no sign of saturation of either the PTV or g_m at high collector biases. This suggests that the only limit to these characteristics is set by the dielectric strength of the barrier layer.

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