**Problem 1.** Write a Verilog model for a synchronous sequence detector. The detector has three inputs and one output. 

*Data_in* is synchronized with the rising edge of the *Clock*. The detector generates *Output* “1” whenever 110 is detected and the other input *Enable* is high.
**Problem 2.** Write a SystemC model (write .h and .cpp) for a synchronous sequence detector. The detector has the following ports:

- **Data_in:** input bit is synchronized with the rising edge of the clock
- **Clock:** Input clock
- **Out1:** generates 1 if “110” is detected
- **Out2:** generates 1 if sequence (3 bits) is equal to the internal bit counter.

Internal 3-bit counter is incremented by 1 on the rising edge of the clock. Assume the counter goes from 000 to 111, and repeats from 000.