

**Department of Electrical and Computer Engineering
State University of New York at Stony Brook**

ESE 555 Advanced VLSI Systems Design (Fall 2009)

CAD Assignment 1: Inverter/Nand/Mux Tutorial

Assignment

Create schematics, symbols, and layouts for an inverter and a 2-input nand gate. Using these symbols and layouts, create a schematic, symbol, and layout for a 2:1 mux using 3 2-input nand gates and 1 inverter. Perform design-rule-checks (DRC) and a layout-vs.-schematic (LVS) check on the layouts of the inverter, 2-input nand, and 2:1 mux. Then, get accurate propagation delays for the 2:1 mux by extracting parasitic capacitances from the layout and simulating the circuit in Spectre.

You probably will not use any of these cells in your final project, so don't be concerned about choosing the "right" cell height or choosing optimal transistor sizes. Try to minimize area and feel free to use all layers available to you. While layout area will be considered in grading, do not spend a lot of time optimizing the layout to save on area.

NOTE:

To use the tool

1. `source cshrc` (from the file in ESE555 page)
2. `source cshrc.cadence` (From the webpage link)
3. `cp /usr/local/cds/ncsu/cdssetup/cdsinit $(YOUR_WORKING_DIR)/.cdsinit`
4. `cp /usr/local/cds/ncsu/cdssetup/cds.lib $(YOUR_WORKING_DIR)/cds.lib`

Description

- Create a directory in your class account called `cad1` and follow the tutorial.
- Make the schematics and symbols for the inverter and 2-input nand. Call the inverter ports `in` and `out`. Call the nand ports `in0`, `in1`, and `out`.
- Follow the guidelines of the tutorial to create layouts for the inverter and 2-input nand. Make sure that you use the same names to label the inputs and outputs of the gates that are used on the symbol. Keep in mind when designing these gates that they will be used in the layout of the 2:1 mux. Examples of things to keep in mind: (1) How will you route between the 4 cells? (2) How will you place the cells to create a 2:1 mux? (3) Where will you place your input and output ports? For example, you could place all your cells in a straight line or in a square. Choose a configuration that minimizes interconnect length.
- Perform a Design Rules Check (DRC) on the layouts of the inverter and nand gates. Save the DRC reports into the files `drc_<component_name>.rep`.
- Perform a Layout Versus Schematic (LVS) on the layouts of the inverter and nand gates. Save the LVS reports to the files `lvs_<component_name>.rep`.
- Make the schematic for the 2:1 mux using the previously designed inverter and nand gates. To instantiate the inverter and nand in the 2:1 mux sheet use the `choose symbol` command from the palette. Use the Navigator to reach the appropriate directory if the inverter and nand are in a different directory from the mux. In this document, the mux will be called `mux2`.
- Perform a Design Rules Check (DRC) on the layouts of the 2:1 mux, saving the DRC report.
- Perform a Layout Versus Schematic (LVS) on the layout of the 2:1 mux, again, saving the report.
- Use Spectre to simulate the circuit in the analog domain. Refer to the inverter tutorial for details as to how to use it. Prior to doing this, add an additional 50fF load on the mux output as described in the tutorial.

Requirements

For the first CAD experiment, you need to prepare the following files:

- ° inverter, 2-input nand and 2: 1 mux schematics and layouts.
- ° Spectre traces for the rise and fall delays for the 2:1 mux (in PostScript format).
- ° DRC report for the inverter, 2-input nand, and 2: 1 mux.
- ° LVS report for the inverter, 2-input nand, and 2: 1 mux.

Deadline

You have to complete the first CAD assignment by Tuesday, September 17, 2009.