

**Department of Electrical and Computer Engineering
State University of New York at Stony Brook**

ESE 555 Advanced VLSI Systems Design (Fall 2009)

CAD Assignment 2: 1-Bit Register

Assignment

To design a register cell.

Description

In this CAD assignment, you will design, layout and simulate a 1-bit register cell, which will be one of the basic building blocks of the register-based modules of your microprocessor project. You may use this cell, or something very similar to it, in circuit blocks such as Instruction Register, Program Counter, Register File, etc.

Implementation

It is often desirable to be able to reset asynchronously the state of the register to a known value (usually zero). An example for a static CMOS transmission gate-based implementation is shown in Fig. 1.

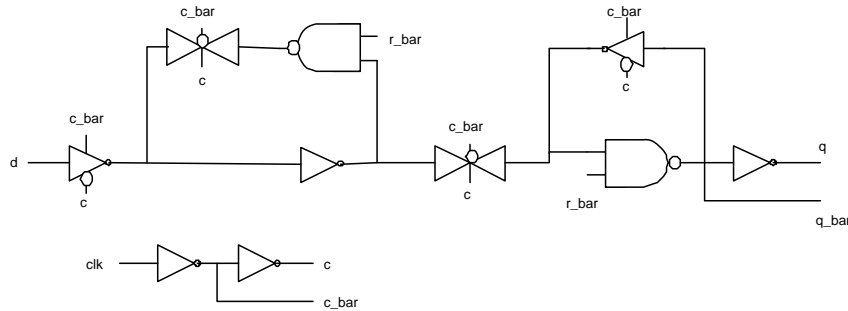


Figure 1: Positive Edge Triggered Flip-Flop Using CMOS Transmission Gates and Clocked Inverters.

The flip-flop could be further compacted by using a dynamic or pseudo-dynamic style with two-phase or single-phase clocking, but we do not recommend these design styles for ESE 555 because they significantly increase the demands on verification in order to assure a working circuit.

Layout Considerations

Since this cell may be a part of your datapath, you should pay careful attention to the layout aspects. Consider this a bit-sliced component with a target bit-slice width (pitch) of 55-60 lambda. If the bit-slice pitch is too small (e. g. 40 lambda), you may find in the future that you don't have enough space to route data buses over top of the datapath.

Procedure

Schematic design

Make a directory called cad2 and do all your work in that directory. Choose the type of flip-flop that you wish to implement, but be sure to make the top-level cell resettable asynchronously to zero and operable with your clocking strategy. Try to optimize size, power, and speed (competing demands) in your design. Create a transistor level schematic of the D flip-flop.

Layout and Verification

When implementing the layout of your cell, you should keep in mind the various layout considerations. While doing DRC and LVS, follow the same procedure as in CAD 1. Be sure to match the ordering of the inputs in your schematic and layout. Save the DRC and LVS reports as `drc_< comp_ name>. rep` and `lvs_< comp_ name>. rep` respectively.

Extract the parasitic capacitances and back annotate those as you did in CAD 1. Save the PEX reports as `pex_lumped_< comp_ name>. rep` and `pex_netlist_< comp_ name>.`

Analog Simulation

Run Spectre on the dff and obtain the rise and fall propagation delay times. Add a capacitance of 50fF to the output node to account for the load capacitance.

Comments

Try to picture how the datapath elements of your processor will fit together (ALU, registers, shifter, etc.). In particular, think about the direction of data flow, the direction of Vdd/Ground routing, and the routing of control lines. Thinking about those issues and pitch-matching ahead of time will make your datapath a more manageable design. On the other hand, don't get to caught up in getting everything correct with this cell.

Requirements

You should have the following:

- Schematics of your D flip-flop with the delays added.
- Layout of the D flip-flop.
- Spectre traces of rise and fall delays for the D flip-flop.
- Spectre output showing minimum set-up and hold times (any less set-up or hold time and the output would be incorrect). This doesn't have to be exact - get within a few picoseconds.
- DRC report.
- LVS report.

Deadline

You need to turn CAD2 in by Thursday, October 6, 2009, 12: 30 pm.