

**Department of Electrical and Computer Engineering  
State University of New York at Stony Brook**

**ESE 555 Advanced VLSI Systems Design (Fall 2009)**

**CAD Assignment 7: Datapath Assembly**

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**Assignment**

To assemble and simulate the pipelined datapath of your microprocessor.

**Description**

The datapath of your microprocessor stores, accesses, and computes the operands of your instructions, and interfaces with the external modules. A good starting point for this assignment would be to look at the data flow for each of your instructions and make sure that you have all the components necessary to do the desired computations. By now, you have designed most of the components needed to achieve the desired functionality. You may need to design tristate drivers and/or muxes. You must decide whether to locate modules on or off of the datapath. For example, you may decide to put the IR and PSR on the datapath. If so, you should design those and incorporate them into your datapath in CAD 7. You must also commit to either a tristate bus or multiplex-or-based design; this decision together with the placement of modules on the datapath dictates the number of buses on your datapath. A natural next step is to assemble all of the modules together and check for correctness. This requires that you present correct control signals to all of the control points in the simulation. (These are input signals, since you do not yet have the control logic.) Be careful to avoid glitches on control signals that might cause incorrect operation.

**Procedure**

With the datapath complete, you should identify critical path and simulate for the worst-case delays. You will have to force control variables and register file select signals by yourself since you do not at present have the de-coder. You will have a lot of control signals to force. Step through each instruction (both Reg-Reg and Reg-Immediate). Pay careful attention to the write-back portion of your "execute" pipeline stage. Be sure there are no glitches on control lines that might cause you to write to the wrong register, or to write bad data.

As part of this CAD assignment, you are also required to define the interface for your chip. List all of the I/O pads on your chip (e. g., address[15:0], data[15: 0], VDD, VSS, etc.), indicating the type (input, output, bi-directional, power) of I/O pad required for each, and giving a short description of each when the function might not be clear from the name. Also, list and describe all of the control signals for the datapath. Your description should include functional specifics for your individual components. You may include a truth-table if you like. This will be needed for the next CAD Assignment.

**Requirements**

Please turn in the following:

- Schematics of the entire datapath.
- Layout of the entire datapath. You may leave any of the unwired points open (e. g., control points). You will have to label those, however.
- List of all the I/O pads with type and description as needed.
- List of all the control signals with descriptions. You may include a truth-table.
- A system block diagram showing the interface between your chip and memory & I/O devices.
- Documentation is important, so make sure you comment your report well. Important considerations that went into the design, and extra features, if any, should be documented.
- Report files (DRC, LVS) for the datapath.

Due November 17