Systematic Development of Analog Circuit Structural Macromodels through Behavioral Model Decoupling

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ABSTRACT

This paper presents a systematic methodology to create customized structural macromodels for a specific analog circuit. The novel contributions of the method include definition of the building block behavioral concept and two original algorithms to generate structural models. Experiments are offered for two-stage opamp and operational transconductor amplifier (OTA) circuits. The automatically produced models are accurate, offer design insight, and require low modeling effort.

Categories and Subject Descriptors

I.6.5 [**Model Development**]: Modeling methodologies

General Terms

Algorithms, Design

Keywords

Analog circuits, Structural macromodel

1. INTRODUCTION

Top-down design has recently emerged as a promising methodology for designing analog circuits and systems [1]. It is more efficient and less costly than traditional, flat design due to its capability to conduct hierarchical optimization at the system, circuit and device level. Hierarchical optimization focuses only on the design variables of a certain level and sets constraints for the next level. For example, system optimization defines the minimum circuit gain requirements that maximize system bandwidth. For high performance applications, however, it was observed that top-down design has serious limitations due to isolating the consecutive design levels. In our experience, even for "mass production" type of applications, like a high precision $\Sigma\Delta$ modulator, system design had to contemplate circuit level details, like circuit noise, maximum input swing and harmonic distortion. Thus, while promising, top-down design cannot be effective unless it considers design attributes of the lower levels too.

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Unlike digital circuits, whose performance is dependent on functionality only, analog circuits exhibit continuous time, nonlinear behavior along numerous performance dimensions. Long and complex transient simulation is needed. For example, analog circuits include many performance specifications, like input offset voltages, maximum swing, distortion, slew rate, noise, and so on. Furthermore, analog circuits consist of strongly coupled stages and devices. As a result, the transient simulation time for larger systems, like a fourth order $\Sigma\Delta$ modulator, becomes very high: about one day is needed to simulate only 50 clock cycles of the modulator behavior. In general, existing solving algorithms for non-linear ordinary differential equations are too slow, and experience many stability or convergence problems. This makes them unfit for system optimization. The alternative to circuit simulation is using detailed system models that integrate realistic circuit models capable of predicting transistor level non-idealities.

Circuit models are of two kinds: structural (physical) and mathematical (black box) models. Please refer to [2] for the most recent advancements in circuit modeling. Structural models offer a qualitative insight into the circuit, and complemented by mathematical models, they express quantitative dependencies between design parameters and performance too. Structural modeling methods, in general, are manual, and they simplify a circuit to the reduced subcircuit that consists only of the dominant devices. Mathematical modeling includes linear and non-linear regression, Volterra series, Pade approximations, wavelet functions, and neural networks [2]. As summarized in Section 2, the most severe limitations of existing modeling methods include poor customization for a certain circuit (which results in poor prediction accuracy), large modeling effort, and limited or no insight into the circuit design. With the exception of [3] - to the best of our knowledge, there are presently no automated techniques for structural modeling.

This paper presents a systematic methodology to create structural macromodels customized for a specific analog circuit. The method takes the transistor structure of the circuit as input, and automatically generates structural models consisting of controlled and independent current and voltage sources, capacitors, resistors and voltage limiters. The produced models express small signal behavior including many circuit nonidealities, like noise and signal clipping. The proposed modeling technique incorporates three novel contributions: (i) Building Block Behavioral (BBB) model concept used to describe the basic building blocks of a circuit, (ii) an algorithm to create Coupled BBB ($CBBB$) models,

and (iii) a decoupling technique to generate Uncoupled BBB (*UBBB*) structural circuit models. The *CBBB* algorithm consists of the steps of grounding the biasing voltages, partitioning the circuit into basic blocks, replacing transistors by their equivalent *hybrid-π* models, and generating the *CBBB* structural model. To expose insight into the circuit and to improve simulation speed, the decoupling method finds the decoupling sequence, and introduces voltage controlled current sources that express all coupling effects. At the end, only input-output dependencies exist in the *UBBB* structural models.

Compared to other methods, the main advantages of the proposed modeling approach are (i) it produces customized models as opposed to fitting a generic model to a specific circuit; (ii) the created models offer insight into the circuit functionality and performance; (iii) models have very good prediction accuracy - comparable to *SPICE* simulation; and (iv) the method requires low modeling effort as designer input and data sampling is reduced. Also, the technique is one of the very few automated structural modeling methods.

The paper has the following structure. Section 2 summarizes related work. Section 3 presents the *CBBB* model and then Section 4 introduces *UBBB* macromodeling. Section 5 discusses our modeling results for two analog circuits. Finally, conclusions are offered.

2. RELATED WORK

Frequency response is one of the main performance characteristics [4, 5]. There are several black box modeling methodologies for AC analysis. Symbolic analysis is arguably the most popular method to analyze circuit systematically [6, 7, 8]. However, it is well known that symbolic analysis is only feasible for small circuits, due to the fact that the number of product terms grows exponentially with the size of the circuits. The approach in [7] partitions the circuit into terminal blocks and middle blocks, where only terminal blocks are analyzed symbolically. By this approximation method, the circuit size that can be analyzed increases dramatically. Also, it is applicable to either loosely or tightly coupled circuits. The method in [8] uses regularities in circuits and symbolic expressions to reduce the size of symbolic expressions.

Behavioral signal path (BSP) technique [9, 10] allows the derivation of design relationships and requirements. It shows all the conversions from voltage to current or vice versa, and how poles and zeros affect the transfer function. This behavioral model gives insight in the operation of a circuit. As limitations, special transformations are needed to capture the transfer function, and BSP model is only suited for linear small signal modeling. Root localization method [3] develops the behavioral model by root sensitivity analysis. It identifies the important nodes in the circuit by calculating nodal sensitivity ratio and coupled nodal sensitivity ratio. Any roots not within one decade of the band of interest are eliminated from the model. This may reduce the accuracy of the model, if the operating frequency changes.

The macromodels proposed in [4] and [11] are simulation-based black box macromodels. They capture both DC and AC features at the transistor-level. The nonlinear behavior is tackled by curve-fitting and piecewise linear (PWL) approximation. These methods are capable of fast time-domain simulation. Parameters of the macromodel are derived from a large number of samples by using curve-fitting

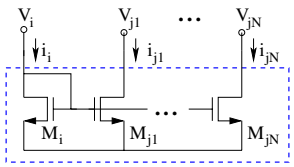

Figure 1: Generic structure of current mirror

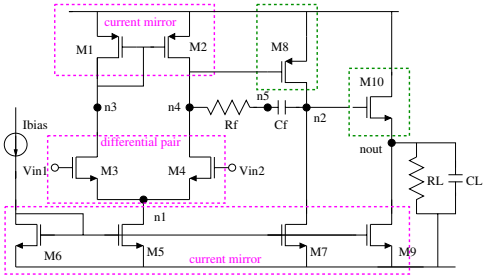

Figure 2: Two-stage Opamp with building blocks

and PWL extraction are from trained NN [11]. These methods have several limitations. A library of well-designed circuits is necessary, and testbenches need to be carefully built in order to get proper design. Finally, simulation-based macromodels are only the simplified equivalent circuit of the transistor-level design in terms of performance. It has very little information about transistor-level trade-offs and constrains, which means that there is no direct mapping from macromodel to circuit parameters.

This discussion arguments that the majority of existing methods are for black box modeling. Hence, in order to capture circuit-level constrains and get insight into the operation of circuits, structural macromodeling is needed. In this paper, customized structural macromodels are developed systematically for a circuit.

3. COUPLED BUILDING BLOCK BEHAVIORAL (CBBB) MODEL

A known fact is that all analog circuits are composed of basic building blocks, such as active load, differential pair, wide-swing current mirror, cascade current mirror, cascode stage, and folded cascode stage [5]. Building blocks are connected directly or by single transistors to realize the required performance. In other words, building blocks appear frequently in all analog circuits, and provide different functionalities. We used this observation to systematically create structural circuit macromodels.

In our modeling approach, first of all, the circuit is decomposed into basic building blocks. All building blocks are modeled separately, and their properties are stored in the library for reuse. Then building blocks are connected together to build the model for the whole circuit. By this way, the models of building blocks are reused. In more detail, the generation of *CBBB* model is as following:

Step 1: Ground all the biasing voltages. In [9] all biasing transistors are removed. Although the role of biasing transistors is to supply the DC current or voltage for the circuit, they also affect the performance of the circuit. For example, the transistors, which supply the biasing current, also connect other transistors to the power supply. The equivalent impedance of biasing transistors appears in the transfer function. Biasing transistors introduce noise to the circuit.

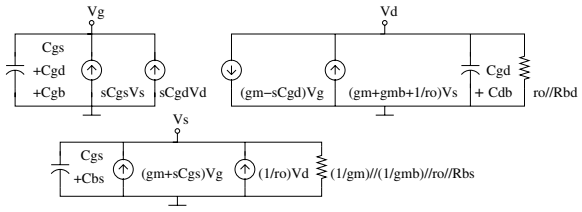

Figure 3: *Decoupled hybrid-π* model for MOSFET

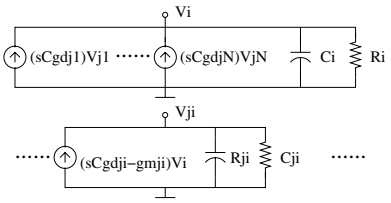

Figure 4: Generic structural model for current mirror

Moreover, they are the link between power supply and other transistors, so they influence the power supply rejection ratio. Therefore, as opposed to [9], the biasing transistors are also considered in our model.

Step 2: Partition the circuit into basic building blocks. The circuit is partitioned by finding the match between the circuit netlist and generic netlist of building block. The generic structure of current mirror is shown in Figure 1. Similar generic structures exist for the other building blocks also. The topology of two-stage opamp is shown in Figure 2. It consists of two current mirrors, one differential pair, one common-source transistor($M8$), and one source follower($M10$) as shown in the figure. The partitioning is shown in the figure.

Step 3: The hybrid-π model is used as the small signal equivalent circuit for MOSFET and BJT. Then, the *hybrid-π* model was transformed to the model we used, called *decoupled hybrid-π* model and shown in Figure 3 . The transformation was done by decoupling all the floating elements. This transformation is error-free.

Step 4: For each building block, replace all the transistors by its decoupled hybrid-π model. The terminal voltages of a building block are independent variables. The current flowing into the terminal is determined by the circuit parameters and terminal voltages. For example, the current mirror of the opamp (Figure 2) is abstracted from the generic structure of the current mirror shown in Figure 4. All the voltages are related to the transistor parameters. All the nodes in the building block are visible from outside, so that all the nodes in the building block can be connected to other nodes in the circuit. This model is the general model for the block.

Step 5: All the building blocks and transistors are put together. Node n_j is said adjacent to n_i if two nodes are the terminals of the same block. For each node, its voltage only depends on the voltages of its adjacent nodes. The voltage v_i of node n_i can be written as

$$v_i = (R_i + sC_i) \times \sum_j (sC_{m_j} \pm G_{m_j})v_j \qquad (1)$$

Where, $(sC_{m_j} \pm G_{m_j})v_j$ denotes the voltage controlled current source ($VCCS$) in block i. R_i and C_i are the total resistance and capacitance associated with node n_i, respectively.

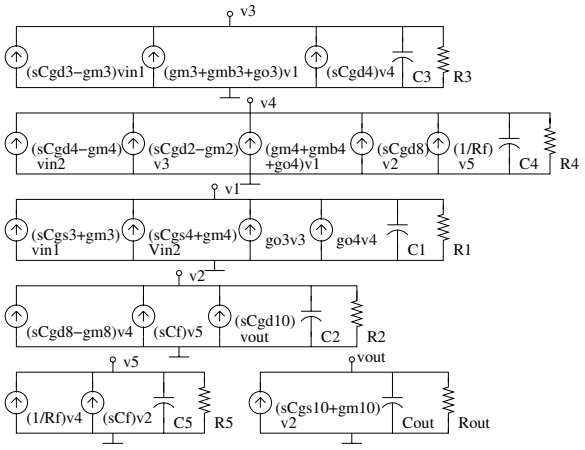

Figure 5: *CBBB* model of Figure 2

The complete *CBBB* model of the two-stage opamp (Figure 2) is shown in Figure 5. We can see that there is a pole at each internal node formed by R_i and C_i. Zeros exist for some $VCCS$s, such as $(sC_{gd3} - g_{m3})v_{in1}$ in the block of v_3.

All the zeros and poles are clearly shown in the *CBBB* model. However, their influence on the transfer function cannot be directly derived due to the coupling between blocks. Also, if the *CBBB* model is used for simulation, the speed is degraded by voltage dependencies. In the next section, we will develop the *UBBB* macromodel by removing all the feedback dependencies in the *CBBB* model.

In general, for the circuit with N nodes, its *CBBB* model is composed of N blocks. The general form of each behavioral building block is shown in Figure 6. It consists of several voltage controlled current sources, loading resistance and capacitance, noise current source, and maximum swing block. Noise current source models thermal noise and flicker noise. The maximum swing block models the clipping effect. We will discuss these nonideal issues in more detail in Section 5.

The advantage of *CBBB* model is that it shows how the nodes are related to circuit parameters. Thus, there is a one-to-one mapping from the original circuit to the *CBBB* model. For example, in order to see how transistor $M3$ is connected in the circuit, we find all the elements in the *CBBB* model which depend on the parameters of transistor $M3$. It turns out that the first two $VCCS$s of block v_3, and the first and third $VCCS$s of block v_1 depend on the parameters of transistor $M3$. By comparing these $VCCS$s with the *decoupled hybrid-π* model, we know that the gate, drain and source of transistor $M3$ are connected to v_{in1}, n_3 and n_1, respectively.

4. UNCOUPLED BUILDING BLOCK BEHAVIORAL (UBBB) MACROMODEL

The proposed solution is to modify the *CBBB* model in such a way that voltage dependencies are replaced by their equivalent functions of the inputs. First of all, the decoupling algorithm defines the decoupling sequence by signal path tracing. Then, the symbolic expression for the voltage that needs to be decoupled is explored from the lower order to higher order. The algorithm for generating *UBBB* model from *CBBB* model is described in detail:

Step 1: Find the decoupling sequence by signal path tracing. We need to find which voltage dependencies should be

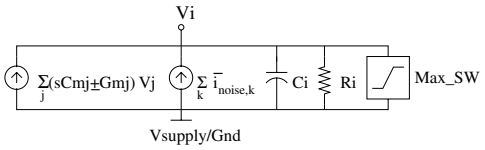

Figure 6: General *CBBB* model with nonidealities

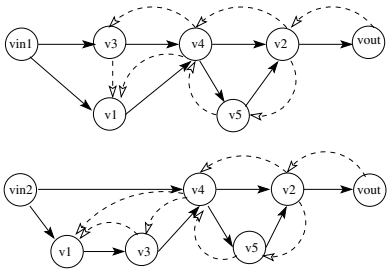

Figure 7: Signal path and feedback dependencies for the circuit in Figure 2

decoupled. For example, in Figure 5, v_3 depends on v_{in1}, v_1, and v_4. While v_4 depends on v_{in2}, v_3, v_1, v_2, and v_5. Obviously, there is a coupling between v_3 and v_4. Hence, we have to determine which voltage should be solved first. We used signal-path tracing algorithm [3] to find the sequence of the nodes in the circuit. As a result, the signal path for Figure 2 is shown in Figure 7. The dotted line represents the feedback voltage dependency, which needs to be decoupled. The modeling sequence follows the signal path from the input to the output as $v_{in1,2} \rightarrow v_1 \rightarrow v_3 \rightarrow v_4 \rightarrow v_5 \rightarrow v_2 \rightarrow v_{out}$.

Step 2: Rearrange CBBB model by the modeling sequence. The feedback dependent voltage v_i was replaced by its equivalent voltage $v_{eq,i}$, as shown in Figure 8, which corresponds to replacing each dotted feedback path by feedforward paths from the inputs in Figure 7.

Step 3: In frequency domain, $v_{eq,i}$ has the general form shown in formula (2)

$$v_{eq,i} = \sum_{p=1}^{P} \frac{a_{i,0} + a_{i,1}s + \cdots + a_{i,n-1}s^n}{b_{i,0} + b_{i,1}s + \cdots + b_{i,n-1}s^n} v_{in,p} \tag{2}$$

Where, P is the number of inputs.

THEOREM 1. *The coefficient of s^i is*

$$a_{i,j} = \sum_t \left((\pm 1) \prod_{k_i k_j} G_{m,k_i k_j}^{\alpha_k} \prod_{l_i l_j} C_{m,l_i l_j}^{\beta_l} \right) \tag{3}$$

Where, α_k,β_l = 0 or 1. G_{m,k_ik_j} is the transconductance between node k_i and k_j. C_{m,l_il_j} is the transcapacitance between node l_i and l_j.

Suppose that there are N nodes in the CBBB model, then

$$\sum_{k=1}^{K} \alpha_k = N - j, \sum_{l=1}^{L} \beta_l = j \tag{4}$$

Where K and L are the total number of G_{m,k_ik_j} and C_{m,l_il_j} in the model, respectively.

For brevity reasons, we did not present the proof.

Step 4: Find the symbolic expression for all the coefficients. This was done in the following steps.

Firstly, only DC parameters are considered by setting $s = 0$. In this case all the capacitors are removed. We only

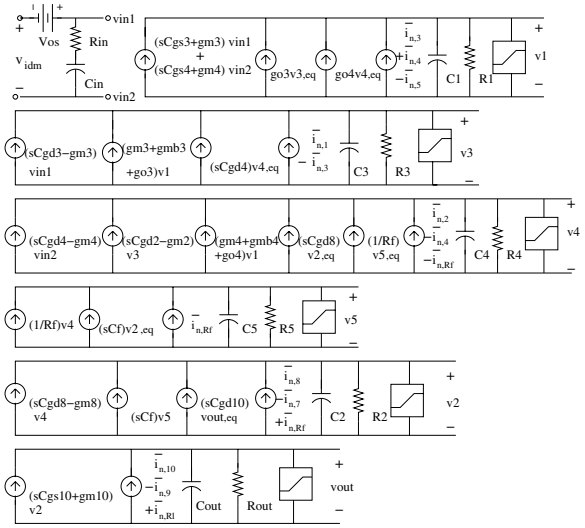

Figure 8: Macromodel for two-stage opamp with nonidealities

replaced one feedback dependency at one time, and kept all the other paths unchanged. For example, we only replace v_3 by formula (5).

$$\frac{a_{0,3}}{b_{0,3}} v_{in1} + \frac{c_{0,3}}{d_{0,3}} v_{in2} \tag{5}$$

Where variables $a_{0,3}, b_{0,3}, c_{0,3}, d_{0,3}$ are determined symbolically by minimizing the *COST* function.

$$COST = \sum_{samples} (\alpha \sum_{i=1}^{N} |\frac{v_{ai,mod} - v_{ai,org}}{v_{ai,org}}| + \beta \sum_{i=1}^{N} |\frac{v_{pi,mod} - v_{pi,org}}{v_{pi,org}}|) \tag{6}$$

Generally, two symbolic expressions are said to be equal if they are numerically equal in the range of interest. In our algorithm, we tried a large number of possible expressions for each coefficient and picked the one that has minimum *COST* over all explored samples. The *COST* function is the accumulated magnitude and phase error over all samples. The exploration of symbolic expressions should meet the constrains defined by the previous theorem. By this way, the exploration space is significantly reduced requiring a reduced number of sample points.

After finding all the coefficients for s^0 term, next step is to find the expression of the coefficients of s. In this step the interested frequency range needs to be swept, and the *COST* function becomes the accumulated error of all samples over the given frequency range. The algorithm for finding symbolic expression for the coefficients of s is shown in Figure 9. The coefficients of higher order term can also be found by the same approach.

Step 5: Replace all the feedback dependencies by its equivalent symbolic functions. The output can be derived by following the signal path. The voltage controlled current sources are functions of the input frequency. Finally, the input stage was added as the first stage, which includes input impedance and offset voltage as shown in Figure 8.

5. TWO CASE STUDIES FOR UBBB MODEL WITH NONIDEALITIES

The frequency response of the *UBBB* model of Figure 2 is shown in Figure 10. It shows that the frequency response

for each voltage v_i that corresponds to
  feedback dependent node n_i
  $COST_i = 0$;
  for $0 < k < iteration_{max}$
    $a_{i,1} = \sum_t (\prod_{ka_i ka_j} G^{\alpha_{ka}}_{m,ka_i ka_j})(\prod_{la_i la_j} C^{\beta_{la}}_{m,la_i la_j})$;
    $b_{i,1} = \sum_t (\prod_{kb_i kb_j} G^{\alpha_{kb}}_{m,kb_i kb_j})(\prod_{lb_i lb_j} C^{\beta_{lb}}_{m,lb_i lb_j})$;
    if $\Sigma_{ka,b}\alpha_{ka,b} = N-1$ and $\Sigma_{ka,b}\beta_{ka,b} = 1$
      $v_{i,eq} = \frac{a_{i,0}+a_{i,1}s}{b_{i,0}+b_{i,1}s}$; ($a_{i,0}$ and $b_{i,0}$ are known)
      for $0 < m < N_{sample}$
        for $f_l < freq < f_h$
          Calculate $COST_i$ from (6);
        end for;
      end for;
      if $COST_i < bestCOST_i$
        $bestCOST_i = COST_i$;
        STORE $a_{i,1}$ and $b_{i,1}$;
  end for
end for

Figure 9: Algorithm for finding the symbolic expression of $a_{i,1}$ and $b_{i,1}$

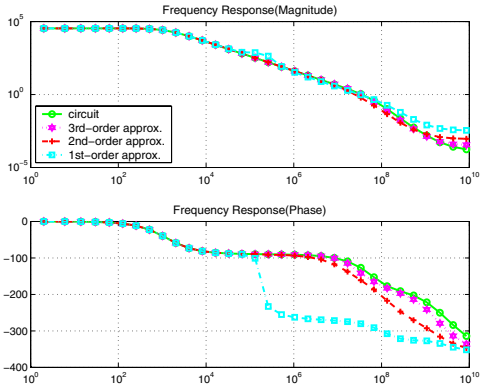

Figure 10: Comparison of frequency response of opamp with $v_{i,eq}$ approximate to s, s^2, s^3

of the structural model is very close to that of the original circuit, if $v_{i,eq}$ is approximated to the third order. If the bandwidth of interest is lower than $100MHz$, the second order approximation is enough. Note that first order approximation, like in most black box models, is very inaccurate.

The results of transient analysis are shown in Figure 11 for small signal, and large signal transient response respectively. Our model has the similar behavior as the original circuit. If input voltage is large, some of the transistors are cutoff, and the output cannot follow the input amplitude. This is modeled by the maximum swing block at each node.

To compare against a recent black box modeling method, the OTA circuit in [14] was modeled by the *UBBB* model, and the generic macromodel in [11]. The frequency responses of two models are very similar. However it took us virtually no effort to produce the structural model, whereas it took one month to build the look-up table for the macromodel in [11].

5.1 Noise

There are four main types of noise mechanisms: thermal noise, $1/f$ noise, generation recombination noise and shot noise [13]. Thermal noise and $1/f$ noise are the dominant

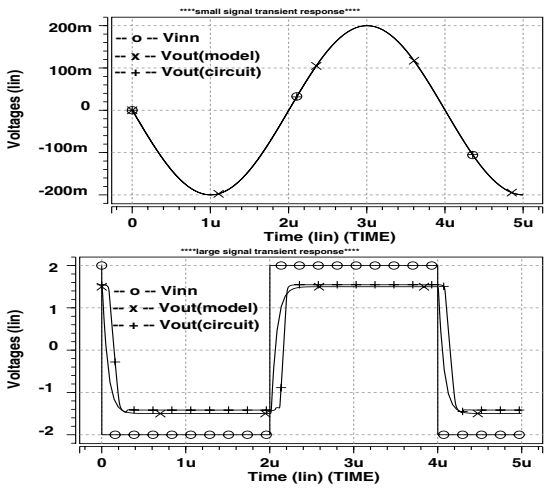

Figure 11: Small signal and large signal transient response for two-stage opamp in a voltage follower configuration (circuit and model)

noise sources in the MOS transistor. The noise current density can be approximated as relationships (7) and (8) for thermal noise and flicker noise respectively [5].

$$\overline{i^2_{n,th}} = \frac{8kT}{3}(g_m + g_{mb} + g_{ds}) \tag{7}$$

$$\overline{i^2_{n,1/f}} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \cdot g^2_m \tag{8}$$

Where, γ is technology dependent, and is about 2/3 for long channel devices, and 2.5 for $0.25\mu m$ MOS devices. In our model, noise current source can be added to each node as shown in Figure 8. To calculate the total output noise, all the input sources were removed, and the symbolic expression of the output noise can be directly derived from Figure 12 without solving equations. The noise current sources in Figure 12 have the general form presented in expressions in (9) and (10):

$$\overline{i^2_{n,i}} = \frac{8kT}{3}(g_{mi} + g_{mbi} + g_{oi}) + \frac{K}{C_{ox}W_iL_i} \cdot \frac{1}{f} \cdot g^2_{mi} \tag{9}$$

$$\overline{i^2_{n,R}} = 4kTR \tag{10}$$

The total output noise in the band from f_l to f_h is the integration of the output noise density over the given bandwidth, which can be approximated as relationship (11).

$$V_{n,tot} = \sum_{k=1}^{k_0} V_{n,out}(f_k) \cdot \frac{f_h - f_l}{k_0} \tag{11}$$

Where $V_n(f_k)$ is the output noise at frequency f_k, and

$$f_k = f_l + (f_h - f_l) \cdot \frac{k}{k_0}$$

The total output noise calculated from the model (in Figure 12) is shown in Table 1. The table gives the comparison between *UBBB* model and the original circuit of opamp in terms of DC gain (A_0), unity gain bandwidth (BW), phase margin (PM) and total output noise ($V_{n,out}$) from $1kHz$ to $100MHz$. The error in A_0, BW, PM, and $V_{n,out}$ are within 0.5%, 5%, 10% and 9%, respectively. This shows that the *UBBB* model works well over a large range of transistor size.

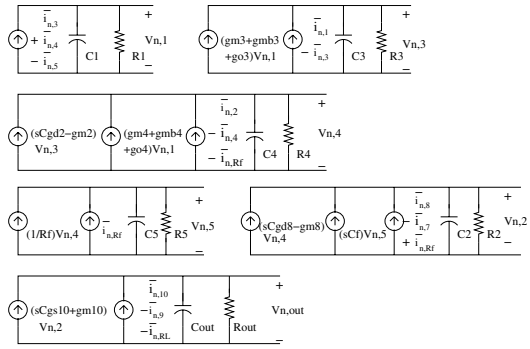

Figure 12: Noise model of two-stage opamp

5.2 Distortion

Distortion is caused by the nonlinear elements in the circuits. In fact, all the transistors, resistors, and capacitors are nonlinear elements that can be described by the nonlinear I/V and Q/V relationships. The *hybrid* π model is the small-signal linear model for the MOS transistor. The nonlinearity of the transistor can be described by the nonlinear transconductance, parasitic capacitance and resistance in the *hybrid* π model, which nonlinearly depend on the terminal voltages [6].

In order to incorporate weakly nonlinearity in our model, all the linear parameters in the *hybrid* π model should be replaced by a higher order nonlinear functions in the close vicinity of the biasing point. As a result, the power of G_{m,k_ik_j} and C_{m,l_il_j} in (4) can be equal to other values besides 0 and 1, similar to posynomial models discussed in [12].

In general, the transistors connected to the node that has the largest swing dominate the distortion of the circuit. If the swing is too large, it may drive the transistor into linear or cutoff region, and this results in voltage clipping. Clipping can be modeled by calculating the maximum swing a node can tolerate, which is set by the DC operating points. In other words, all the transistors should be in the right operation region in order to give the proper performance. The maximum swing the node can tolerate is equal to $min(V_{max} - V_0, V_0 - V_{min})$, where V_{max} and V_{min} is the highest and lowest voltage the node can reach without clipping , and V_0 is the DC operating voltage of the node. The maximum swing function for Figure 2 can be expressed as expression (12). The clipping effect of our model is shown in Figure 11.

$$\begin{cases} V_b - V_{ss} - V_{Tn5} < V_1 < V_{in1} - V_{Tn3} \\ max(V_b - V_{ss} - V_{Tn7}, V_{out} + V_{Tn10}) < V_2 < |V_{Tp8}| + V_4 \\ max(V_4 - |V_{Tp2}|, V_{in1} - V_1 - V_{Tn3}) < V_3 < V_{dd} - |V_{Tp2}| \\ max(V_2 - |V_{Tp8}|, V_{in2} - V_1 - V_{Tn4}) < V_4 < min(V_{dd} - |V_{Tp8}|, V_3 + |V_{Tp2}|) \\ min(V_4, V_6) < V_5 < max(V_4, V_6) \\ V_b - V_{ss} - |V_{Tp9}| < V_{out} < V_2 - V_{Tn10} \end{cases} \quad (12)$$

6. CONCLUSION

This paper presents a systematic method to produce structural macromodels customized for a specific analog circuit. The novel contributions include (i) building block behavioral model concept, (ii) an algorithm to create *CBBB* models, and (iii) a decoupling method for generating *UBBB* models. Nonidealities like noise and distortions are also modeled. Experiments are offered for two-stage opamp and OTA circuits. Produced models offer insight into the circuit, error is at most 10% compared to *SPICE*, modeling effort is minimal.

sample		A_0 [dB]	BW [MHz]	PM [°]	$V_{n,out}$ $[mV]$
1	circuit	84.1	32.1	42	8.56
	model	84.1	32.3	40	9.12
2	circuit	82.6	32.3	43	7.82
	model	82.5	32.0	47	8.65
3	circuit	52.5	24.8	54	1.16
	model	52.5	24.5	59	1.28
4	circuit	85.2	38.9	42	9.29
	model	85.2	37.3	48	9.16
5	circuit	48.9	34.9	47	3.62
	model	48.9	34.5	50	3.89
6	circuit	85.5	32.2	42	9.60
	model	85.5	32.0	47	10.02

Table 1: Performance comparison for opamp of different sizing solutions

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