Systematic Methodology for Designing Reconfigurable $\Delta\Sigma$ Modulator Topologies for Multimode Communication Systems

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Abstract

This paper proposes a methodology for designing reconfigurable continuous-time $\Delta\Sigma$ modulator topologies. The methodology is based on the concept of generic topology that expresses all possible signal paths in a reconfigurable topology. Topologies are optimized for minimizing the complexity of the topologies, maximizing the sharing of circuitry for different modes, maximizing the topology robustness with respect to circuit nonidealities, and minimizing total power consumption. The paper presents a case study for designing topologies for a three mode reconfigurable $\Delta\Sigma$ modulator, and compares topologies with state-of-the-art design.

1. Introduction

With the emergence of new wireless communication standards, the circuitry in future personal wireless communication systems must support multiple operating modes, such as AMPS, GSM, CDMA, WCDMA, and UMTS [1, 2, 3]. A promising trend is to use reconfigurable receiver-on-a-chip that meets the resolution and bandwidth requirements of different communication standards [4]. In this approach, a main task is developing high performance, compact multimode analog to digital converters (ADC), in which the circuit netlists for different modes share as many analog cells as possible [1].

Reconfigurable multimode ADCs have two main advantages as compared to having a collection of single-mode ADCs: (1) Reconfigurable ADCs are much more compact [1]. Thus, occupy less area. (2) Design time, hence cost, is reduced. In reconfigurable ADCs, many blocks are shared between different modes. Therefore, the total design effort is less.In the future, reconfigurable ADCs might be used in software controlled reconfigurable communication systems (software radio) that graciously adapt to new communication standards and performance constraints.

There is few work on reconfigurable multimode ADCs [1, 2, 3, 4]. Work is mostly on reconfigurable continuous-time $\Delta\Sigma$ modulators due to their power efficiency, superior linearity at low bandwidths, and inherent bandwidth resolution tradeoff in the noise-shaping characteristic. So far, the design of reconfigurable multimode $\Delta\Sigma$ modulators is manual and relatively unsystematic. There is little understanding on how to develop optimal reconfigurable topologies for a new set of modes. Also, to improve design closure and reduce cost, topology design must contemplate a fair amount of circuit nonidealities. Existing techniques are either customized to a few single-mode topologies [5, 6], or consider ideal systems without any nonidealities [7, 10]. More efficient methodologies are needed for systematically designing reconfigurable ADCs while contemplating nonidealities early in the design flow.

This paper proposes a systematic methodology for designing reconfigurable continuous-time $\Delta\Sigma$ modulator topologies. Topologies are optimized for minimizing the complexity of the topologies, maximizing the sharing of circuitry for different modes, maximizing the topology robustness with respect to circuit nonidealities, and minimizing total power consumption. These are important requirements for real applications. The methodology is based on the concept of generic topology that expresses all possible signal paths in a reconfigurable topology. We present the modeling of generic topologies including four types of nonidealities: (1) integrator related, (2) quantizer related, (3) feedback DAC related , and (4) circuit related nonidealities. Models are used in the methodology to set up a set of nonlinear equation sets. Equations are solved for finding efficient reconfigurable topologies. Found topologies are then refined using *Simulink* simulation of models with more detailed nonidealities.

The paper is organized as follows. Section 2 summarizes related work. Section 3 is on modeling of modulator nonidealities for design. Section 4 presents the proposed topology design methodology. Section 5 discusses the case study. Finally, conclusions are offered.

2. Related work

There is currently no work on methodologies for systematic design of reconfigurable $\Delta\Sigma$ topologies. Existing

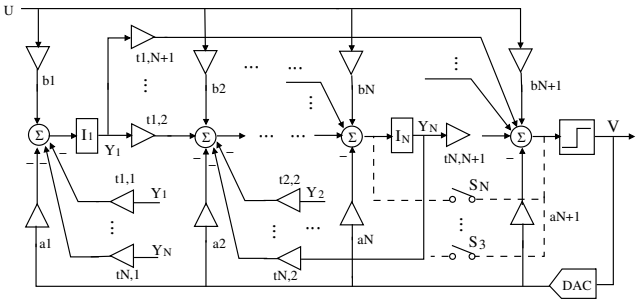

Figure 1. Reconfigurable topology

research [1, 2, 3, 4] presents design cases, but no methodology is introduced.

Current design methodologies are for single-mode ΔΣ only. Most of the work is on topology parameter optimization with limited modification of the modulator topology. Medeiro *et al.* [5] propose a design flow based on extensive analysis and modeling of the nonidealities that degrade the ΔΣ modulator performance. However, their methodology is limited to the four single-mode, discrete-time topologies supported by CAD tools – SDOPT and FRIDGE. Francken *et al.* [6] describe an approach for high-level simulation and synthesis of discrete-time ΔΣ modulators. Behavioral models for integrators, quantizer, and feedback digital-to-analog converter (DAC), are integrated in a synthesis tool (DAISY) that selects the modulator topology with the lowest power consumption for a given specification and constraints for the building blocks. An analytical integration method for the simulation of continuous-time ΔΣ modulators is suggested in [8]. However, the set of allowed topologies is not complete, thus optimal solutions might be missed. Tang and Doboli [7] present a synthesis algorithm that finds the optimal topology for a given specification by solving a mixed-integer nonlinear programming (MINLP) problem with a cost function expressing the signal path complexity, sensitivity, and power consumption of the topology. This method considers only single-mode ΔΣ modulators built out of ideal blocks.

Design methodologies for single-mode ΔΣ modulators cannot be directly used for developing reconfigurable multimode ADCs, because they lack any capability of conducting global optimizations across the multiple modes. Hence, while solutions might be optimal for each mode, they are hard to be integrated into a reconfigurable ADC that shares as many blocks as possible between its different modes.

3. Modeling for reconfigurable topology design

This section presents the system and circuit models used in reconfigurable ΔΣ modulator topology design. The design methodology is discussed in Section 4.

3.1. Generic reconfigurable topology

As shown in Section 4, reconfigurable ΔΣ modulator topologies are designed starting from a generic topology. The generic topology contains all possible signal paths in the reconfigurable modulator. The generic topology is shown in Figure 1. Blocks I_1 to I_N are nonideal integrators.

The state-space description of the generic topology is expressed as equations (1) and (2):

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} = \left(\begin{bmatrix} -t_{1,1} & -t_{2,1} & \cdots & -t_{N,1} \\ t_{1,2} & -t_{2,2} & \cdots & -t_{N,2} \\ \vdots & \vdots & \ddots & \vdots \\ t_{1,N} & t_{2,N} & \cdots & -t_{N,N} \end{bmatrix} \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} + \begin{bmatrix} b_1 & -a_1 \\ b_2 & -a_2 \\ \vdots & \vdots \\ b_N & -a_N \end{bmatrix} \begin{bmatrix} U \\ V_t \end{bmatrix} \right) \cdot \begin{bmatrix} I_1 & & \\ & I_2 & \\ & & \ddots \\ & & I_N \end{bmatrix} + \begin{bmatrix} N_{th1} \\ N_{th2} \\ \vdots \\ N_{thN} \end{bmatrix} \quad (1)$$

$$V = \begin{bmatrix} t_{1,N+1} & t_{2,N+1} & \cdots & t_{N,N+1} \end{bmatrix} \begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_N \end{bmatrix} + \begin{bmatrix} b_{N+1} & -a_{N+1} \end{bmatrix} \begin{bmatrix} U \\ V_t \end{bmatrix} + E_q \quad (2)$$

And,
$$V_t = V + N_j \quad (3)$$

Where, U and V are the input and output of the modulator, respectively. Y_i is output of i^{th} integrator. E_q is the quantization noise. a_i denotes the path from the feedback DAC to the input of the i^{th} integrator, b_i is the path from the input signal to the input of the i^{th} integrator, and $t_{i,j}$ represents the path from the output of the i^{th} integrator to the input of the j^{th} integrator.

By solving the state-space equations, the transfer function of the modulator is written as (4) [9]:

$$V = L_0 U + L_1 V + E \quad (4)$$

Variables L_0 and L_1 are loop filters, which can be symbolically derived from the state-space equations, similar to [7].

The proposed state-space description is different from the one used in [9], in the sense that four kinds of nonidealities are captured: (1) I_i is the nonideal transfer function for the i^{th} integrator. (2) $N_{th1}, \cdots, N_{thN}$ denote the circuitry noise in each integrating stage. (3) N_j accounts for the jitter noise in the feedback DAC. (4) Also, the nonlinearity can be modeled by calculating the transfer function at the harmonics of the input signal. By incorporating nonidealities in the state-space description of the generic topology, their impact on the modulator performance can be derived as closed form expressions, and thus tackled early in the design flow.

We discuss next circuit nonideality modeling.

3.2. Modeling of circuit nonidealities

We grouped the circuit nonidealities into four categories: (1) integrator related, (2) quantizer related, (3) feedback DAC related, and (4) circuit related nonidealities.

I. Integrator related nonidealities

Finite gain and bandwidth was modeled by including finite gain (A_{0i}) and poles/zeros (p_{i1}, p_{i2}, z_{i1}) in the transfer function I of the integrator, as shown in equation (5):

$$I_i = A_{0i} \frac{1 + s/z_{i1}}{(1 + s/p_{i1})(1 + s/p_{i2})}, \quad i = 1, \cdots, N \quad (5)$$

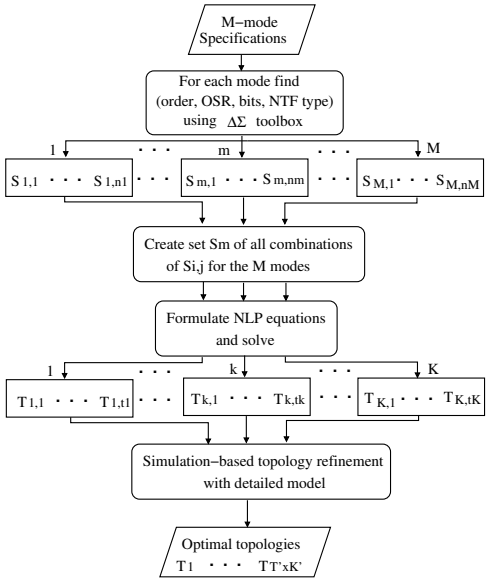

Figure 2. Reconfigurable ΔΣ topology design flow

Notice that the NTF only depends on loop filter L_1. Therefore, minimizing the variation of the NTF is equivalent to minimizing L_1. Suppose the integrator is ideal ($I_i = 1/s$), then L_1 for N^{th} order modulator can be written as equation (6):

$$L_1 = \frac{c_{n,N}s^N + \cdots + c_{n,1}s + c_{n,0}}{c_{d,N}s^N + \cdots + c_{d,1}s + c_{d,0}} \tag{6}$$

Coefficients $c_{i,j}$ are the symbolic function of the coefficients $x_{m,i}$ for the signal paths.

If the first integrator is replaced by equation (5), then the order of L_1 becomes to $N+1$, and can be expressed as:

$$\widetilde{L_1} = \frac{\tilde{c}_{n,N+1}s^{N+1} + \tilde{c}_{n,N}s^N + \cdots + \tilde{c}_{n,1}s + \tilde{c}_{n,0}}{\tilde{c}_{d,N+1}s^{N+1} + \tilde{c}_{d,N}s^N + \cdots + \tilde{c}_{d,1}s + \tilde{c}_{d,0}} \tag{7}$$

To minimize the difference between $\widetilde{L_1}$ and L_1, the following function $h_{m,k}$ was added to the overall cost function (13) used in design:

$$h_{m,k} = \sum_{n=0}^{N} \left(\left| \frac{\tilde{c}_{n,n+1} - c_{n,n}}{c_{n,n}} \right| + \left| \frac{\tilde{c}_{d,n+1} - c_{d,n}}{c_{d,n}} \right| \right) + |\tilde{c}_{n,0}| + |\tilde{c}_{d,0}| \tag{8}$$

II. Quantizer related nonidealities

For topology design, the quantization noise is assumed to be white noise [9]. The comparator offset and hysteresis are considered when simulating the modulator, as shown in Figure 3.

III. Feedback DAC related nonidealities

With jitter noise, the modulator transfer function (4) becomes $\tilde{V} = L_0U + L_1\tilde{V} + L_1N_j + E$. $\tilde{V}$ is the output of the nonideal modulator.

Since the coefficient of jitter noise N_j is L_1, which is set by the design parameters $(order, OSR, bit, NTFtype)$ of the modulator. Therefore, the effect of clock jitter cannot be minimized by optimizing the signal paths.

IV. Circuit related nonidealities

Circuit noise is modeled as white noise, as in equation (1). The noise of all the integrating stages is

$$\tilde{V} = L_0U + L_1\tilde{V} + \sum_{n=1}^{N} \left(\frac{c_{n,N}s^N + \cdots + c_{n,1}s}{L_{1,den}} \times N_{th,n} \right) + E \tag{9}$$

Variable $L_{1,den}$ denotes the denominator of the ideal loop filter function L_1, and $c_{n,i}$ is the symbolic coefficient of s^i for stage n. Therefore, the following term in the cost function (13) captures the circuit noise

$$h_{m,k} = \sum_{n=1}^{N} \sum_{i=1}^{N} |c_{n,i}| \tag{10}$$

Nonlinearity can be modeled by calculating the frequency responses at different harmonic frequencies. The goal is to minimize the variation in L_1 in the presence of harmonic distortion. For example, let assume that only the second order nonlinear component (k_2) of the first stage is considered. We represented the frequency response at $2s_0$ of the ideal and nonlinear modulator by $\widetilde{L_{1,o2}}$ and $L_{1,o2}$, respectively:

$$\widetilde{L_{1,o2}} = \frac{L_{1,o2,num} + k_2\left(\sum_{i=1}^{N-1} c_{n,i}s_0^i\right)}{L_{1,o2,den} + k_2\left(\sum_{i=1}^{N} c_{d,i}s_0^i\right)} \tag{11}$$

Hence, the term in the cost function (13) is

$$h_{m,k} = \sum_{i=1}^{N-1} |c_{n,i}| + \sum_{i=1}^{N} |c_{d,i}| \tag{12}$$

4. Methodology for design of reconfigurable ΔΣ modulator topology

Reconfiguration of a modulator may occur at three levels: (1) topology reconfiguration, (2) topology parameter reconfiguration, and (3) cell circuitry reconfiguration [4]. The proposed reconfigurable topology design methodology focuses on the first two reconfiguration levels, as well as deriving the design requirements for the cell circuitry reconfiguration. The design goal for the reconfigurable ΔΣ modulators is to (1) minimize the complexity of the reconfigurable topology, (2) increase the robustness of the system with respect to circuitry nonidealities, and (3) minimize total power consumption.

The design flow in shown in Figure 2. It consists of two steps: (1) topology synthesis by NLP solving, and (2) topology refinement by simulation of the detailed modulator model. The steps are discussed next.

4.1. Topology design based on NLP solving

The input to the topology design methodology is a set of M specifications for the M-mode reconfigurable ΔΣ modulator. For each target specifications, such as dynamic

range (DR), a set of solutions that can achieve the target DR are found by using the ΔΣ toolbox [10]. Each solution has four parameters: (i) the order of the loop filter, (ii) the over sampling ratio (OSR), (iii) the internal quantizer bits, and (iv) the NTF type. The order of the loop filter ranges from 2 to 5, and OSR is chosen from the set $\{16,24,32,40,56,64,80,96,112,128\}$ due to the implementation constraints of the decimation filter. Internal quantizer bits range from 1 to 6. In our experiment, only single bit quantizer was considered, due to its inherent linearity and ease of implementation. The NTF type can be Butterworth or inverse Chebyshev. Then, the $n^{th}(0 \le n \le N)$ solution for the $m^{th}(1 \le m \le M)$ mode can be written as $S_{m,n} = (order, OSR, bit, type)_{m,n}$. Theoretically, any solution for a single mode can be combined with the solution for another single mode to build a multimode ADC.

Then, a set of possible candidates for the M-mode reconfigurable ADC are generated by combining M design parameters for each of the M modes, each of which can be written in the form $S_k = S_{((m_1,n_1),(m_2,n_2),\cdots,(m_M,n_M))_k}$. Each candidate can be implemented using different topologies, and optimal topologies are generated by the proposed methodology.

For a given set of parameters $(order, OSR, bit, type)$, the corresponding NTF is calculated by the ΔΣ toolbox [10]. Lets assume that the signal transfer function (STF) is unity, and the loop filters $L_{0,d}$ and $L_{1,d}$ are calculated from NTF and STF [9], which are then transformed into the s-domain. Then, the desired continuous-time loop filter functions $L_{0,c}$ and $L_{1,c}$ are produced.

Next, symbolic expressions for $L_{0,c}$ and $L_{1,c}$ of the loop filter are derived from the state-space equations of the generic topology. By equating the symbolic and numerical coefficients of $L_{0,c}$ and $L_{1,c}$, for an M-mode reconfigurable continuous-time ΔΣ modulator, lets suppose that the order of the m^{th} mode is N_m, then there are in total $\sum_{m=1}^{M} 3\times(N_m+1)$ equations with $\sum_{m=1}^{M}(N_m+1)\times(N_m+2)$ unknowns. For a cost function f, the reconfigurable topology design problem can be formulated as

$$\begin{gathered} \textit{minimize cost } f = f(x_{m,i}, wx_{m,i}); \\ \textit{subject to: } g(x_{m,i}) = 0; \\ \textit{subject to: } x_{m,i} \ge 0,\ wx_{m,i} \in \{0,1\}; \end{gathered}$$

Unknown $x_{m,i}$ denotes any of the unknown coefficient a_i, b_i, and $t_{i,j}$ for the m^{th} mode. Unknown $wx_{m,i}$ denotes whether the signal path with coefficient $x_{m,i}$ is present or not. g are the $\sum_{m=1}^{M} 3\times(N_m+1)$ equality constrains obtained from equating symbolic $L_{0,c}$ and $L_{1,c}$ to the desired loop filter functions for all M modes.

The used cost function is

$$f = \alpha_1 \sum_m \sum_i wx_{m,i} + \alpha_2 \sum_{m_1} \sum_{m_2 \ne m_1} \sum_{i,j} |wx_{m_1,i} - wx_{m_2,j}|$$

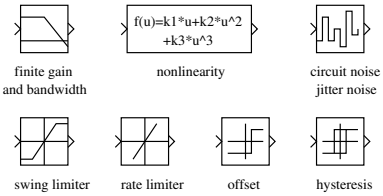

Figure 3. Nonideal blocks in Simulink

Mode	Dynamic Range (bits/dB)	Channel Bandwidth
UMTS	11.5/70	1.92MHz
CDMA2000	13/80	615kHz
GSM	15/90	190kHz
EDGE	14.5/87	270kHz

Table 1. Design specifications

$$+\sum_m \beta_m \Big(\sum_k \gamma_{m,k} \cdot h_{m,k}(x_{m,i})\Big) \tag{13}$$

The first two terms represent the topology complexity of the modulator: the first is the absolute complexity (considering the total number of signal paths in the topology) and the second is the relative complexity (accounting for the changes of signal paths when the modulator is reconfigured). $wx_{m_1,i}$ and $wx_{m_2,j}$ are the binary value of the corresponding signal paths in the two modes (0 if the path is not present and 1 if the path is present). The second term attempts to maximize the circuit sharing between modes.

The third term minimizes the sensitivity of the modulator with respect to circuitry nonidealities. $h_{m,k}$ is the function of $x_{m,i}$ that minimizes the impact of nonidealities on NTF. As explained in Section 3, four kinds of nonidealities are formulated in this function. Experiments show that this term is crucial to the performance of the final topologies.

By formulating the topology synthesis problem as MINLP and including the above four nonidealities into the cost function, a set of topologies, (each of which is optimal solution for the particular candidate $T_k = T_{((m_1,n_1),(m_2,n_2),\cdots,(m_M,n_M))_k}$), are generated.

4.2. Simulation based topology refinement

In this step, the reconfigurable topology is tuned based on more detailed simulation. Hence, only local optimization is conducted. *Simulink* models showed in Figure 3, are used in this step. First, the modulator is scaled, such that the voltage swings at the output of each integrator are within a certain range. Then, all nonidealities discussed in Section 3 are simulated in *Simulink*.

Power consumption is estimated from two considerations. On one hand, power consumption of each integrating stage is proportional to the unity-gain bandwidth (e.g., G_m/C_k) of the integrator. On the other hand, power consumption is proportional to the biasing current of the circuit, which has to be large enough to suppress the nonlinearity of the transconductor into required range. This relationship is analyzed in detail in [11]. As a result,

Order	OSR		
	UMTS	CDMA2000	GSM-EDGE
2	96	128	–
3	48	64	96
4	40	48	64
5	28, 32	40	48

Table 2. Design parameters

complexity	3 single modes	[1]	*opt1* (5-5-5)	*opt2* (5-4-4)	*opt3* (5-4-3)
N_p	39	17	22	20	21
$N_{p,r}$	–	6	10	11	14
$N_{c,r}$	–	11	12	9	7
$N_{c,r2}$	–	0	9	6	4
$N_{c,r3}$	–	11	3	3	3
$N_{p,a}$	39	39	39	33	31
η_d	–	28.2%	24.4%	33.3%	33.3%
η_p	–	0%	0%	15.4%	20.5%

Table 3. Design complexity

$P \sim (K_{p1}(G_m/C_k), K_{p2}/HD_{3,k})$. The power consumption of the reconfigurable $\Delta\Sigma$ modulator is estimated by the sum of the power consumption of active circuit cells, like transconductors and integrators, for all the modes.

Finally, a set of optimal solutions are generated in terms of topology complexity, robustness, and power consumption. Meanwhile, the design requirement for each building block is also derived.

5. Case study: Reconfigurable $\Delta\Sigma$ modulator topology for multimode communication system

[1] discusses a state-of-the-art multimode continuous-time $\Delta\Sigma$ modulator. Table 1 summarizes the bandwidth and dynamic range specifications for the different modes. We compared the systematically generated topologies with the one in [1]. We noticed that the DR requirement for GSM-mode and EDGE-mode are very close (0.5 bit). We merged the GSM-mode and EDGE-mode into a single mode, considering that different bandwidth requirements can be achieved by modifying the sampling frequency. So, three different DR/BW specifications for the three modes were used as input to the design flow in Figure 2.

Next, the possible design parameters for each mode was

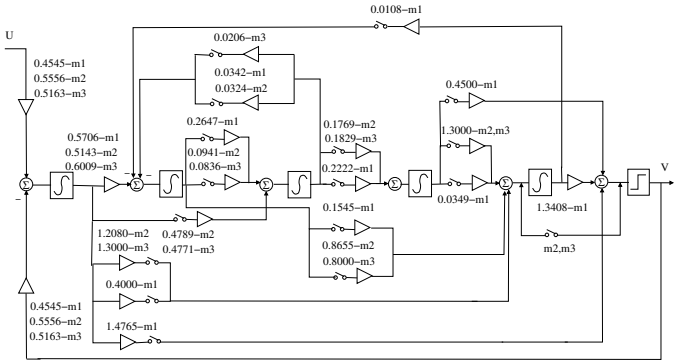

Figure 4. Reconfigurable topology *opt2*

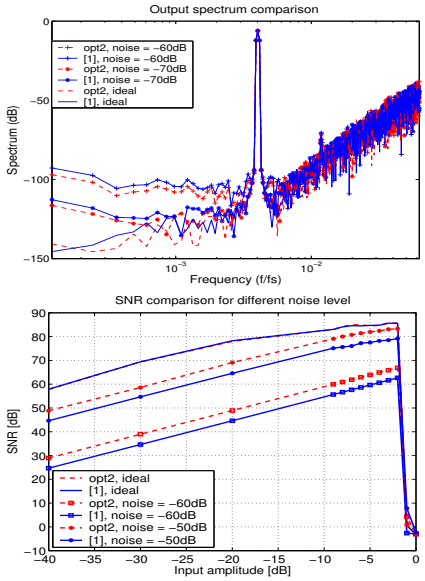

Figure 5. Output spectrum and SNR degradation by circuity noise for topology in Figure 4 and [1]

produced, as shown in Table 2. The table gives the OSR requirements for different orders of the modulator in order to achieve the DR specification. In total, 60 possible combinations of design parameters were generated for the three modes.

Then, all optimal topologies were found by NLP solving. All the optimal topologies were passed to the next step, where detailed, nonideal models are used. The modulator was simulated and scaled. Finally, several optimal topologies were produced. One of the optimal topologies is shown in Figure 4.

Table 3 presents the comparison between three of the optimal solutions and the topology in [1], as well as a non-reconfigurable topology that includes three single mode modulators. The comparison is in terms of the topology complexity and design effort. Topology *opt1* has order 5 for all its three modes, while topology *opt2* and *opt3* have order $< 5,4,4 >$ and $< 5,4,3 >$ for the three modes, respectively. The complexity of the system is analyzed from number of signal paths (N_p), the number of non-reconfigurable cells ($N_{p,r}$), and the number of reconfigurable cells ($N_{c,r}$). It can be seen that reconfigurable ADC are much more compact than the three single mode architecture. Also, the complexity of the produced topology is very similar to the state-of-the-art design in [1].

Assume that the design effort of designing a two-mode and three-mode reconfigurable cell is $1.5\times$ and $1.8\times$ that of designing a non-reconfigurable one, respectively. Then, the reduction in estimated design effort (η_d) as compared to the non-reconfigurable case (in which an M-mode modulator is built by simply connecting M single modes), can be

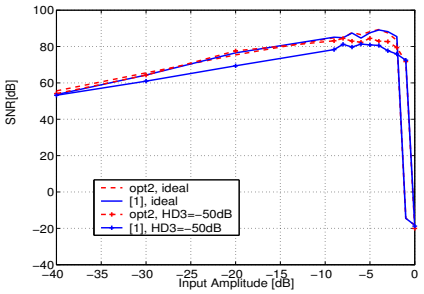

Figure 6. SNR degradation due to HD3 for topology in Figure 4 and [1]

estimated as equation (14):

$$\eta_d = 1 - \frac{1.5 \times N_{c,r2} + 1.8 \times N_{c,r3} + N_{p,r}}{N_{p,non}} \qquad (14)$$

The result is shown in Table 3. It shows that topology *opt2* and *opt3* have the highest design effort reduction (about 33.3%), because they contain least number of signal paths as well as reconfigurable cells.

The estimated power consumption reduction (η_p) is calculated from the sum of the power consumption of active building blocks for each mode [6]. The total number of active paths for all three modes is shown in table 3. The generated optimal topology *opt2* and *opt3* show improvement (up to 20%) in power consumption compared to the topology in [1].

In order to analyze the robustness of the produced topologies, we simulated the CDMA2000-mode of topology *opt2*. Figure 5 is the output spectrum and SNR comparison of the two topologies with different levels of circuitry noise. Figure 5 shows that the circuitry noise whitens the in-band noise, and the higher the noise density the higher the noise floor and the lesser the SNR. We can see that the topology in [1] is more sensitive to this effect. As a result, the SNR degrades $3dB$ more for topology in [1], if the noise level equals to $-60dB$, and $5dB$ more for noise of $-50dB$ compared to the topology *opt2*.

Figure 6 shows the performance degradation caused by third order harmonic distortion (HD3) in the first integrating stage. We can see that again the generated topology is more robust than the topology in [1]. SNR drop is reduced by $3dB$ in the case of $-50dB$ HD3.

6. Conclusion

This paper presents a systematic methodology for designing topologies for reconfigurable continuous-time $\Delta\Sigma$ modulators. To the best of our knowledge, this is the first attempt for systematically designing reconfigurable $\Delta\Sigma$ modulators. The design methodology includes following sequence of steps: system-level design parameter exploration for the multiple design specifications, topology design based on solving nonlinear equations expressing four kinds of circuit nonidealities (finite gain and bandwidth, circuitry noise, distortion and clock jitter) and topology refinement using simulation of more detailed circuit nonidealities, like comparator offset and hysteresis, integrator slew rate and maximum swing limit.

Our case study for designing a 3-mode reconfigurable $\Delta\Sigma$ modulator showed that reconfigurable ADCs is less than $1/3$ of a design of 3 single mode modulators. Also, the estimated saving in power consumption for reconfigurable $\Delta\Sigma$ modulator can be as large as 20% of that of the 3 single mode approach. The reconfigurable topologies produced using our methodology requires less reconfigurable cells than a recent state-of-the-art reconfigurable $\Delta\Sigma$ design [1]. Finally, our reconfigurable topologies are more robust to circuit noise and third order harmonic distortion than the reconfigurable $\Delta\Sigma$ design in [1].

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