Lab 6 Sequence Detectors

1. Objectives

For this lab you will design a sequence detector using two types of finite state machines: Moore type and Mealy type.

2. Preliminary Lab

The requirements for a finite state machine with one input (X) and one output (Z) are as follows. If two consecutive zeros (00) or ones (11) are observed on the input X, then the output Z is asserted high. Otherwise, the outputs are both low.

In this prelab, you will

1. Design a Moore type finite state machine implementing the above specifications using D flip-flops. Specify the circuit using viewdraw and verify its operation using viewsim.

2. Design a Mealy type finite state machine implementing the above specifications using J-K flip-flops. Specify the circuit using viewdraw and verify its operation using viewsim.

3. Compare the schematics and simulation results. What are the differences in cost (number of gates, flip-flops) and performance of the two implementations? Are the simulation results identical?

You need to show your complete prelab work including schematic and simulation results to the TA at the beginning of this lab.

3. Circuit Implementation

In the lab, you will build two circuits designed in the prelab and verify their operation.

1. Build a Moore type finite state machine using D flip-flops. Show its operation to the TA.

2. Build a Mealy type finite state machine using J-K flip-flops. Show its operation to the TA.
4. Checkoffs

To save yourself (and the TA) time, complete all the sections below, then have the TA examine your work.

1. Prelab (Show your work (including circuit diagrams) to the TA)
   TA: __________________________ (30%)

   TA: __________________________ (20%)

   TA: __________________________ (20%)

4. Turned In On Time
   TA: __________________________ (full credit (100%))

5. Turned In One Week Late
   TA: __________________________ (1/2 credit (50% x Points))